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Adoption and Use of Multimedia and Interactive Games for Instructional Purposes in Nigerian Secondary Schools – the Case of "Lainos World"

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ABSTRACT
A report on the survey of user perception of an educational computer game in some Nigerian schools. Electronic games have become increasingly popular among adolescents and young adults in Nigeria in recent times due to improved access to the computer, the internet, the mobile phone and other technological devices and services. As such, it is believed that computer games could be integrated into the educational system to enhance the teaching and learning processes. A study was conducted in the Lagos area, on the preparedness of teachers and secondary school students to utilize computer games in education. A multimedia and interactive system was developed which offers instructional geopolitical knowledge on all sovereign countries while engaging the user in a virtual reality game mode as well as traditional windowed application tutor and quiz modes. This was equally assessed by the select schools as to its effectiveness and motivational values. The product (Lainos World[SM]) was adjudged as innovative and beneficial by the vast majority of the participants. Several issues affecting the implementation and successful adaptation of educational computer games are outlined.

Keywords - Games, Educational Computer Games, Secondary Schools, Teachers, Students, Perception

1. INTRODUCTION

There are different software categories such as operating systems, development environments, security utilities, office productivity tools, games, educational, etc. Initially games were developed for special machines (arcade, consoles, etc.) but were ported and proliferated after the emergence of the affordable personal computer. Computer games evolved from Mazes, Tetris and Space Invader variants to more challenging types such as Chess and Scrabble. A recent trend within the last decade is edutainment software, which combines entertainment (games, music, video, etc.) with educational material presentation..

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Most of the products in this new category are in the form of tutorials, puzzles, etc. WordRescue® by Apogee Software® in 1992 was a successful early edutainment package for learning English words [1]. Children and other adolescent gamers have long been interested in Three Dimensional Virtual Reality and Role Playing Games (3D VR & RPG), a genre popularized by ID Software® through their products *Wolfenstein 3D* and *DOOM*® released in 1992 and 1993 respectively [2]. In this type of game, the user assumes a role and transverses a multimedia, virtual environment to accomplish a goal. Unfortunately, most games in this category contain increasing violent content. They have become a source of concern to parents and the developed world after some high school firearms shooting and, killing incidents were linked to addiction to such games [3, 4].

2. RELATED WORKS

Recent research by Virvou et al [5, 6] has shown that the educational effectiveness of games on children is enhanced when 3D VR & RPG is incorporated. They reported case studies based on classroom evaluations of VR-ENGAGE, a game which was designed to teach geography to primary school children.

The player had to navigate a castle and search for a 'book of knowledge' by answering geography questions to open doorways. It was demonstrated (statistically established) that student groups generally expressed greater interest and performed better with VR-ENGAGE than was obtained using a traditional windows GUI for the same geographical study and test questions. They also offered tips on what is required for commercial success of such an application. Interactive Parables® [7] is an early commercial product along this line.

Adeosun [8] suggested application of cybernetic pedagogy to the Nigerian education system through the design and use of educational games. It was reported [9] that Nigerian teachers-in-training who would be the ones to inculcate computer skills into the learners (at primary and Junior secondary school level) still needs a lot of education themselves especially in the areas of the capabilities of computer games for learning. Studies in Lagos and Benin [10] shows that computer games are played mostly by boys in Nigeria for several reasons; parental attitude encourages that girls be kept busy while boys are allowed to play, sibling attitude when boys think that girls cannot really play and would rather play with dolls; innate attitude when girls are just not interested or think perhaps that the games are macho. Also the perception exists that games are designed for boys with the preponderance of fighting, shooting and violence. Thus the need for a gender-neutral, educational game has been long established in the Nigerian environment. Given all the above, the author was encouraged to develop a multimedia educational and entertaining computer game titled Lainos World.

3. METHODOLOGY

3.1 LAINOS WORLD Software

The application is a localizable, scalable, E-rated, interactive, 3D VR & RPG that offers multimedia tutoring on all sovereign countries. It is a game of strategy which facilitates a virtual tour to access interesting national features such as boundary shape, map, flag, currency, monument, local time and national anthem. The tour sequence, duration and total distance traveled is used to compute a player's final score so that apart from learning about the countries or answering quiz questions, a competitive goal exists, which is to make the shortest one-way tour of a region or the entire world within the shortest possible time interval. Unlike in VR-ENGAGE where the user wanders round a castle looking for a key, in LAINOS WORLD he or she seeks and must touch the flag/currency of a nation in Virtual Reality mode in other to exit to another country. Multimedia format was utilized to enhance cognition. Walker et al [11] reported that studies have shown that voice messages may be more effective than written ones. Similarly, Asan [12] showed that in Turkey, even Teacher education is enriched by multimedia content over traditional approaches.

LAINOS WORLD Properties (Systems Analysis)

i) *Localizable* implies the product is designed to be easily adaptable for several languages using Resource Compilers.
ii) *Scalable* implies the product is extensible and, the application rules are totally separated from the data.
iii) *E-rated* implies that by Entertainment Software Rating Board standards, the product would be for everyone i.e. has content that is suitable for ages 6 and older. In addition to this, in LAINOS WORLD, the sex of the game character can be selected or hidden.
iv) *Interactive* implies program responds to user activity which itself is governed by strategies to master and control unfolding game scenario(s).
v) *Multimedia* implies the use of appropriate text, pictures, music, voice, etc. to convey messages. Sound can be turned off/on in LAINOS WORLD based on user preference.
vi) *Tutoring* implies factual, accurate geo-political descriptions and quiz about various territories/countries.
vii) *Game of Strategy* means it is not dependent on chance alone but also on strategic planning. This is because the user seeks to make the shortest one-way tour of world regions within minimal duration. Sources of motivation for the game include the novel '*Around the World in Eighty Days*' by Jules Verne and the open-ended '*Traveling Salesman Problem*' of combinatorial optimization

LAINOS WORLD Features

i) World Atlas presented as political maps that may be Zoomed or Panned with relevant geopolitical details (Name, Capital, Total Area, Population, Time Zone, Telephone Calling Code Internet Top Level Domain, Location, Currency, Independence, National Day Religions, Official Languages, Capital's Geographical Co-ordinates) on 210 countries
ii) Country identifier on world map tutor
iii) Geographical distance calculator between countries' capitals
iv) Country locator on map quiz
v) Three dimensional (3D) virtual tour of the world or desired regions with walls shaped as actual national boundaries
vi) Multimedia [text & speech] instructor for geopolitical narrator or national capitals' quiz

vii) Instrumental music of national anthems
viii) National maps showing major cities and boundary nations
ix) National flags, monuments and currencies
x) Local date/time announcer
xi) Customizable as to User preferences and inclusion of custom notes and images

Screenshots of the application are shown in Figure 1.0 and Figure 2.0 contrasting the display of Nigeria's geopolitical information details via different formats

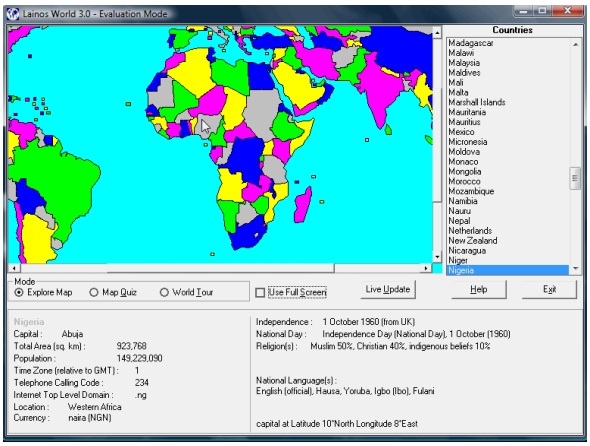

Figure 1.0: LAINOS WORLD Windowed mode showing Nigeria's geopolitical information

Figure 2.0: LAINOS WORLD Virtual Reality mode showing a female tourist in Nigeria

3.2 Research Methods

Survey research studies were conducted in the Lagos area. The entire Senior Secondary school students in Lagos and their Instructors are the target population. The aims are:

1. To investigate the perception of teachers and students concerning the use of educational computer games in the classroom.
2. To ascertain the motivational and educational values of LAINOS WORLD in a classroom setting.

The study area covers three educational zones namely Ikeja, Ojo and Ibeju-Lekki. Three private Senior Secondary schools were used due to availability of computers and prompt cooperation of the school heads, attributes that are not as forth-coming in public schools. Thus Cluster sampling was utilized to get the schools and students while purposive sampling was utilized to select the instructors (of Geography, Computer Studies and Social Studies). The Sample consists of eight (8) instructors and thirty three (33) Senior Secondary Two (SS2) students selected from each school. The mean age of the students in each school is 16 years. Three research assistants (fresh graduates) were trained and appointed to assist in the administration of questionnaires and to assist with installation and demonstration of LAINOS WORLD software. They were always available to observe and assist the class teachers.

3.3 *Data Collection and Analysis*

The data were collected over a two week period, with the questionnaire addressing the first objective administered on the first day while the other was treated a fortnight later after exposure to LAINOS WORLD. Two students were also randomly selected for interview alongside the class teacher after the completion of both questionnaires. The Microsoft Excel® software was used for descriptive statistical analysis such as calculation of means, percentages and plotting of Pie charts. The studies have inherent limitations for certain due to the fact that:

1. The validity is dependent on the honesty on the respondents
2. The participants' perceptions may change over time due to alterations in their exposure and experiences, repeatability may gradually degrade.
3. Although the researcher made efforts to standardize the procedure, there may have been variations in the way the research assistants conducted the experiments (treated the participants) at the different locations.

4. RESULTS AND DISCUSSION

Our findings follow from an analysis of respondent data. The results are shown in Figures 3 to 6.

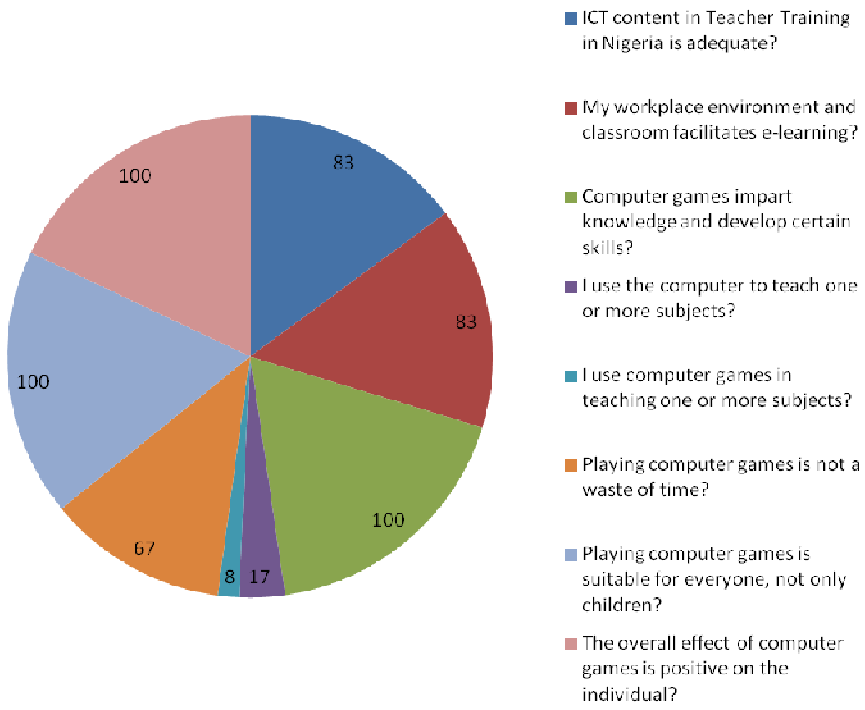

Figure 3.0: Perceptions on use of ICT and games generally (% of Instructors Who Agree)

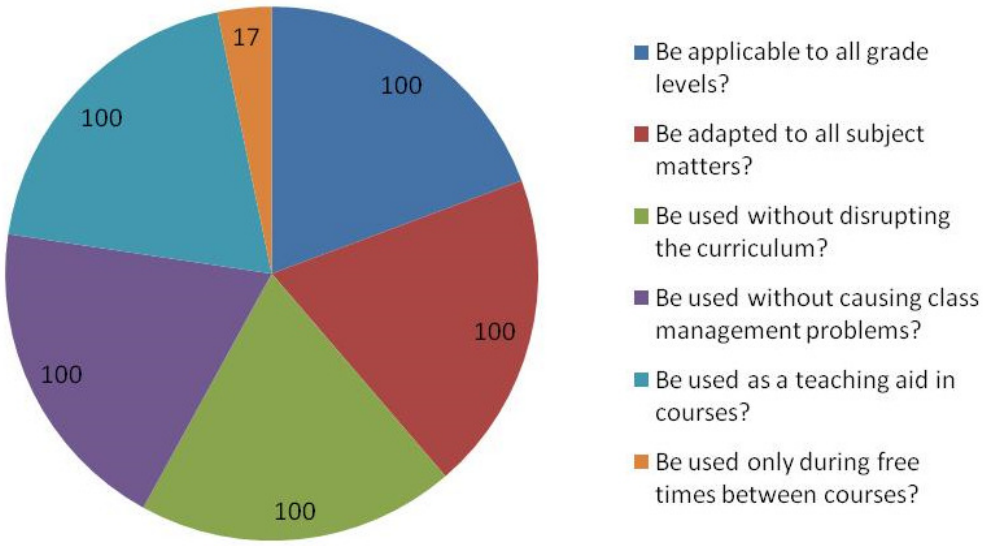

Figure 4.0: Perceptions on computer games with educational features (% of Instructors Who Agree)

Surprisingly, majority of the instructors believe that the current content of ICT in Teacher education in Nigeria is adequate (Figure 3). This contrasts sharply with earlier reports as stated in the introduction review. Most agree that while there is availability of computers in their work place, these are hardly used in teaching but for administrative and other duties. Although about two-thirds of the teachers support computer gaming in general as presently constituted, they are all agreed on the need to adapt them to education and incorporate such into the curriculum at all levels (Figure 4).

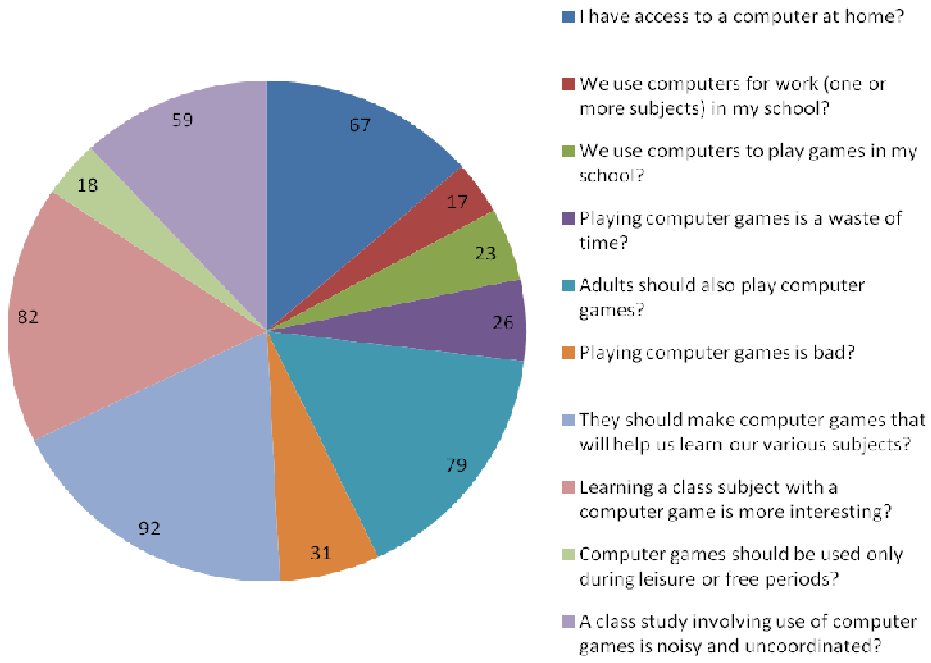

Figure 5: Perceptions on use of computer games in education (% of Students Who Agree)

From Figure 5, the interpretation is that students generally have access to computer at home (67%) and also in private schools mostly for recreational rather than educational purposes. They are however eager to have computer games with educational values relating to their actual subjects.

They also show higher concerns about class management issues than the teachers who believe such situation can be easily handled. This probably explains why the students expect that even educational

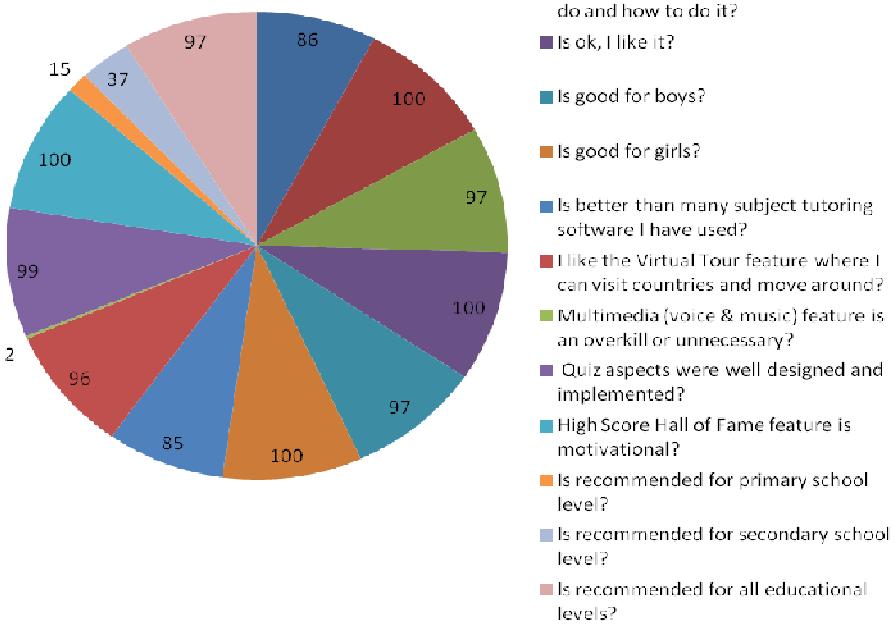

Figure 6: Perceptions on LAINOS WORLD software (% of Students Who Agree)

From Figure 6, there is a consensus (86%) among the students as to the ease of use of LAINOS WORLD. They all liked it (100%) irrespective of gender. The virtual reality aspect and multimedia features are appreciated by over 96% of participants and make the product preferred over other tutoring programs they have previously encountered.

The quiz and scoring features are particularly found inspirational (100%). Also, the students believe that LAINOS WORLD could be used by all educational levels thus confirming the E-rating design goal.

While most of the perceptions about gaming and LAINOS WORLD are positive, the interview revealed other issues such as:

1. Computer games could be time engaging due to the innate compulsion to top the 'High Score Chart.'
2. Educational computer games will help develop other skills (reasoning, memory, etc.) aside the motor skills improved by normal games.
3. There are relatively few educational computer games in the market compared to the other gendre.
4. Multimedia, VR games like LAINOS WORLD have special computer specification requirements and may not run smoothly on old system configurations which still abound in developing countries.
5. Teacher responsibility is increased in coordinating use of educational computer games since a student may proceed at self-pace in game usage, also the adaptation of testing (quiz) features in games for subject examination need to be explored.

5. CONCLUSIONS

This work has highlighted the Senior Secondary school teachers' and students' perceptions of the use of educational computer games, based on surveys carried out in Lagos, Nigeria. It established their desire and willingness to adopt such games and the fact that available computers are presently being used for administrative and recreational purposes only in our secondary schools. The study also found that students are very receptive to the LAINOS WORLD program and found it both educational and motivational. The instructors however, express concerns about infrastructures for massive deployment of educational games.

6. FUTURE DIRECTIONS

The researcher is conducting a more extensive research on the use and impact of ICT on Lagos secondary schools which employs hypothesis testing. Global studies are also on-going to determine LAINOS WORLD's effect on students' test performance scores in Geography, particularly of their knowledge about various countries.

REFERENCES

[1] 3DRealms, 2009. "Word Rescue", Retrieved February 4, 2009 from http://www.3drealms.com/word/index.html

[2] Wikipedia, 2010. "ID Software". Retrieved March 27, 2010 from http://en.wikipedia.org/wiki/Id_Software

[3] BBC News |Health|, 2000. "Video games 'increase aggression' ", Retrieved August 24, 2010 from http://news.bbc.co.uk/1/hi/health/70707.stm

[4] The Sun, 2005. "COURTING VIOLENCE: Researchers link video games to aggression in boys", Retrieved August 24, 2005 from http://www.sunnewsonline.com

[5] Virvou, M., Katsionis, G. & Manos, K., 2005. "Combining Software Games with Education: Evaluation of its Educational Effectiveness." *IEEE Journal of Educational Technology & Society* 8(2), pp. 54-65.

[6] Virvou, M., Manos, C., Katsionis, G. & Tourtogglou, K., 2002. "VR-ENGAGE: A Virtual Reality Educational Game that Incorporates Intelligence." Pp. 339-342, *Proc. of IEEE Conference on Advanced Learning Technologies*, September 16-19, 2002, Kazan, Russia.

[7] GraceWorks, 2003. "The Interactive Parables". Retrieved July 25, 2010 from http://www.graceworksinteractive.com/games.html

[8] Adeosun, O. V., 1996. "Towards more effective delivery of instruction in Nigeria: the cybernetic approach", *Research in Curriculum Studies* 1(1), pp. 103-108.

[9] Aremu, A., 2004. "Knowledge of the educational implications of computer games by some student teachers in Southwest Nigeria". *The Nigerian Journal of Guidance and Counseling* 9(1), pp. 16-24

[10] Ulomata, T.T., 1996. "Computer Games and Nigerian Children: The Effect of Socialization on Girls' Choice of Careers in Computerization". Presentation at the 8th International Conference of the Gender and Science and Technology Association, Ahmedabad, India. Available and retrieved March 4, 2010 from http://archive.wigsat.org/gasat/46.txt

[11] Walker J.H., Sproull, L. and Subramani, R., 1994. "Using a Human Face in an Interface." *In Proceedings of ACM Conference on Human Factors in Computing Systems*, CHI'94 pp. 85-91

[12] Asan A., 2003. "School experience course with multimedia in teacher education: an example from Turkey". *Journal of Computer Assisted Learning* 19(1), pp. 21-34

AUTHOR'S BRIEF

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Traffic Control and Resource Management for ATM Networks Using Explicit Rate-Based Scheme

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ABSTRACT
Asynchronous Transfer Mode (ATM) is an electronic digital data transmission technology that could transport real time transaction, video conference and audio as well as image files, text and email. Its performance has become extremely important in view of their ever expanding usage, and the complexity of their functions. However one of the fundamental challenges facing broadband information transportation is to determine congestion control strategies to support multiple classes of traffic in the ATM based networks. In this paper, we highlights major issues of ATM network problems and presents an architectural model that enables open and flexible network control and high utilization of network resource that can sustain quality of service for all connections. Specifically this paper provide a general overview of congestion control mechanisms and present a generic, fast transient cell rate algorithm for ATM Networks.

Keywords: ATM Networks, Traffic Control, Resource Management, Multiplexed, Congestion Control

1. INTRODUCTION

ATM is an electronic digital data transmission technology implemented as a network protocol, developed in the mid 1980's. Two groups, the International Telecommunications Union and the ATM Forum were involved in the creation of the standards. ATM is a packet switching protocol that encodes data into small fixed-sized cells (cell relay) and provides data link layer services that run over OSI Layer 1 (physical links).

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ATM exposes properties from both circuit switched and small packet switch networks making it suitable for WAN networking as well as real-time media transport [13,1]. The basic objective of traffic control strategy in an ATM network is to enable high utilization of network resources to sustain an acceptable quality of service (QOS) for all connections. However the bursty nature of the ATM traffic imposes strict requirements for traffic control. Hence there is need for more sophisticated traffic control resource management actions. Traffic control methods can be divided into two categories: reactive control and preventive control.

Reactive control methods regulate the traffic flow at the access points based on current traffic levels within the network, while preventive control methods provide a fair allocation of bandwidth by requiring at times of high network load, that each connection's traffic flow remains within specified bounds appropriate for the supported service [3].

Several works on congestion control in ATM Networks has been reported in literature. Feedback schemes are a widely studied research area for congestion control.

A closed-loop feedback control mechanism was used in [2], that allow the network to control the cell emission process at each source. The feedback control mechanisms predefined thresholds are used as indexes to detect network congestion. Therefore, the queue length is chosen as a criterion to detect congestion. When the queue length exceeds a certain threshold, the congestion control is triggered by reducing the source rate. However, to define the threshold we have to consider the characteristics of the traffic sources and their Quality of Service (QQS) requirements as well as the buffer size, which is a complicated task.

Explicit congestion mechanism for ATM Networks' using an Artificial Neural Network to predict the traffic arrival patterns was proposed in [14]. The predicted data rate in conjunction with the current queue information of the buffer is used to generate a value that will inform the source to reduce its transmission rate. The results of a simulation study are presented which suggest that the mechanism provides a simple and effective traffic management for ATM networks. Cell loss due to congestion shows a 5 to 10 times improvement compared with the static approach.

Neural network for Call Admission Control (CAC) based on the Probability-RAM (pRAM) neuron model was presented in [7]. Because pRAM neural networks can be implemented in hardware easily, they make excellent controllers in the ATM environment. The performance of controller was analyzed through simulations, and the results are compared with the equivalent capacity of CAC algorithm. The result shows that the proposed hardware-based controller guarantees the required quality of service and at the same time provides an improvement in network utilization.

Based on the emerging standards for Broadband Integrated Services Digital Networks (B-ISDN), ATM offers the economically sound "bandwidth on demand", features of packet-switching technology at the high speeds required for today's LAN and WAN networks and tomorrow's. The basic problem of ATM network is the statistical behaviour of the cell arrival process, where at a buffer; cells generated at several different sources are multiplexed together. It has been found that the qualities of service parameters, such as jitter and loss probability are very sensitive to the assumed source characteristics [11].

Therefore, there is need for more sophisticated traffic control model to enable high utilization of network resources and performance. In this paper, fundamental challenges facing broadband information transportation were identified.
An architectural model that enables open and flexible network control and high utilization of network resource using explicit rate-based scheme is proposed. The intention is to determine congestion control strategies to support multiple classes of traffic in the ATM based networks.

2. ATM NETWORKS AND SERVICE CATEGORIES

ATM networks are connection-oriented; two systems on the network can only communicate if they inform all intermediate switches about their service requirements and traffic parameters. This is similar to the telephone networks where a circuit is setup from the calling party to the called party. In ATM networks, such circuits are called Virtual Circuits (VCs).

The connections allow the network to guarantee the quality of service by limiting the number of VCs. Typically; a user declares key service requirements at the time of connection setup, declares the traffic parameters and may agree to control these parameters dynamically as demanded by the network. Based on the type of the traffic and the quality of service desired, ATM applications can use one of these service categories [8]:

- Constant Bit Rate (CBR): This category is used for emulating circuit switching and the cell rate is constant. Examples of applications that can use CBR are telephone, video conferencing, and television (entertainment video).

- Variable Bit Rate (VBR): VBR allows user to send at a variable rate. Statistical multiplexing is used and so there may be a small non-zero random loss depending upon whether or not the application is sensitive to cell delay variation. This category is subdivided into two categories: Real time VBR (rtVBR) and Non-real time VBR (nrtVBR). For non-real time VBR, only mean delay is specified, while for real time VBR, maximum delay and peak-to-peak Cell Delay Variation (CDV) are specified. An example of real time VBR is interactive compressed video while that of non-real time VBR is multimedia email.

- Available Bit Rate (ABR): This category is designed for normal data traffic such as file transfer and email. Only ABR traffic responds to congestion feedback from the network.

- Unspecified Bit Rate (UBR): This category is designed for those data applications that want to use any left-over capacity and are not sensitive to cell loss delay. Examples of applications that can use this service are email, file transfer, news feed e.t.c. Of these, ABR is most commonly used service category. It allows ATM networks to control the rates at which delay-insensitive data sources may transmit.

3. TRAFFIC CONTROL CAPABILITY AND CONGESTION FUNCTIONS

ATM network is expected to have the following traffic control capabilities; Network resource management, connection admission control, usage parameter control and network parameter control, priority control, traffic shaping and congestion control [10].

3.1. Network Resource Management

A tool of network resource management which can be used for traffic control is the virtual path technique. By grouping several virtual channels together into a virtual path, other forms of control can be easily simplified.

3.2 Connection Admission Control

Connection admission control (CAC) is the set of actions taken by the network during the call set up phase to establish if a virtual path or virtual channel can be accepted by the network. It is a procedure for determining whether a connection request is admitted or denied. A connection can only be established if sufficient network resources are available to establish the connection end-to-end with the required quality of service. This connection allows the network to guarantee the quality of service by limiting the number of connections. The procedure is based on resource allocation schemes applied to each link and switching unit.

3.3 Usage Parameter Control and Network Parameter Control

Usage Parameter Control (UPC) and Network Parameter Control (NPC) do the same job at different interfaces. The UPC function is performed at the user node interface, while the NPC function is performed at the network node interface. The main purpose of UPC/NPC is to protect the network resources from malicious as well as unintentional misbehaviour which can affect the quality of service of other already established connections.

Once a connection has been accepted by the connection admission control (CAC), the Usage Parameter Control (UPC) monitor and control traffic at the network entrance to determine whether the traffic conforms to the traffic contract. The UPC is referred to as traffic policing.

3.4 Priority Control

ATM cells have an explicit cell loss priority bit in the header so that at least two different ATM classes can be distinguished. A single ATM connection can have both priority classes when the information to be transmitted is classified into more and less important parts.

3.5 Traffic Shaping

Traffic shaping actively alters the traffic characteristics of a stream of cells on a VPC or VCC in order to reduce the peak cell rate, limit the burst length or reduce the cell delay variation by suitably spacing cells in time.

4. ANALYSIS OF CONGESTION CONTROL SCHEMES

Congestion is a state in which traffic or control resource overload is not able to guarantee the negotiated quality of service to the established connections and to the new connection requests. Congestion is critical in both ATM and non-ATM networks. When two burst arrive simultaneously at a node, the queue lengths may become very resulting in buffer overflow. At the points where the total input rate is larger than the output link capacity, congestion becomes a problem. Congestion can be caused by unpredictable statistical fluctuations of traffic flows or network fault:

$$sum(Input\ Rate) > Available\ link\ capacity$$

Most congestion control scheme consists of adjusting the input rates to match the available link capacity. One way to classify congestion control schemes is by layer of ISO/OSI reference model at which the scheme operates. For instance, there are data link, routing, and transport layer congestion control schemes.

Typically, a combination of these schemes can be used. The selection depends upon the severity and duration of congestion [2]. The best method for networks that are almost congested is to install higher speed links and redesign the topology to match the demand pattern.

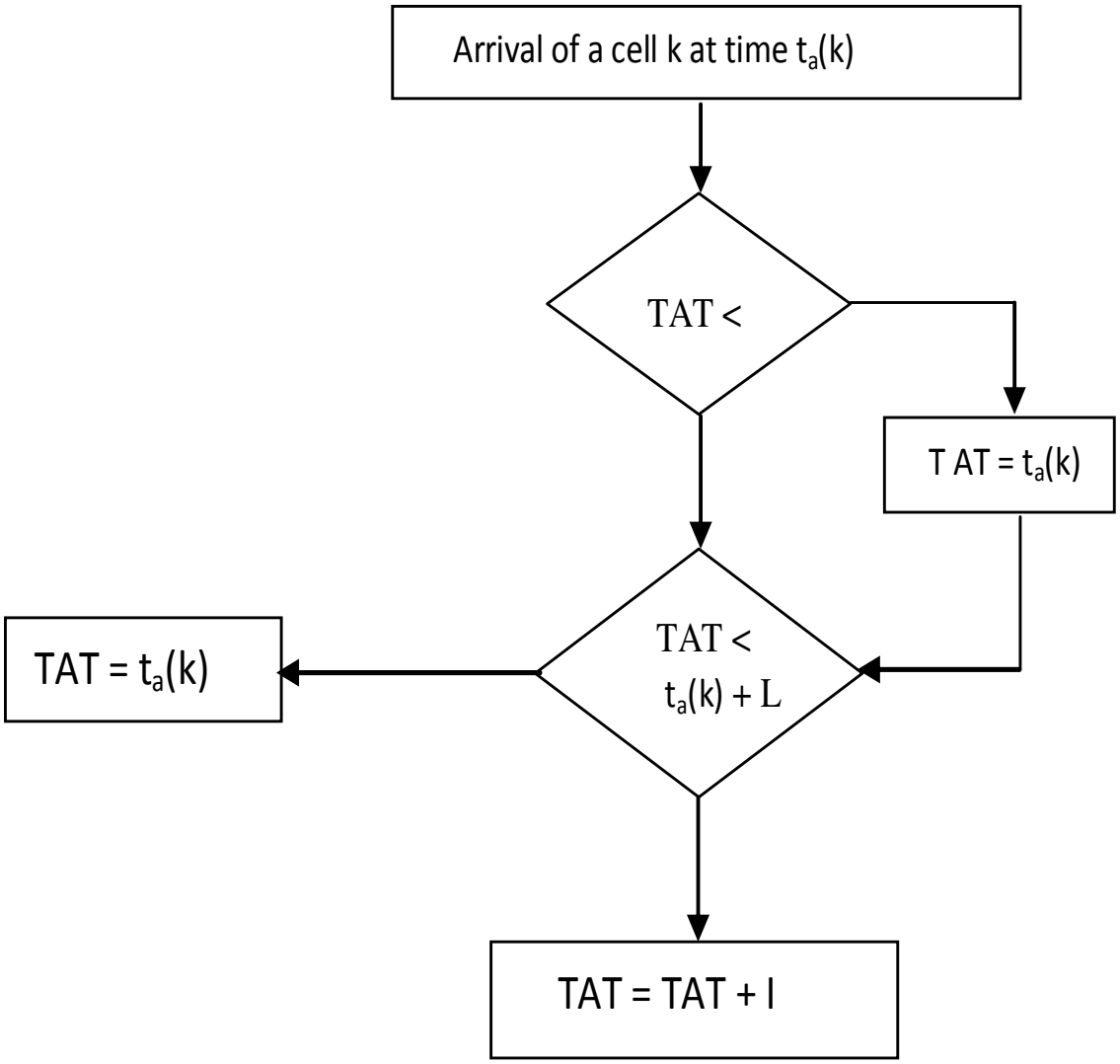

Fig. 1 - The Generic Cell Rate Algorithm (GCRA)

For sporadic congestion, one method is to route according to load level of links and to reject new congestion if all paths are highly loaded. This is called Connection Admission Control (CAC). For congestions lasting less than the duration of connection, an end-to-end control scheme can be used. For example, during connection setup, the sustained and peak rate may be negotiated [8].

4.1 Generic Cell Rate Algorithm (GCRA)

Generic Cell Rate Algorithm (GCRA) is an algorithm defining conformance with the traffic parameters containing in the traffic contract. Using appropriate descriptors. GCRA is also called "leaky bucket" algorithm, which is used to enforce regularity in the arrival times. Basically, all arriving cells are put into bucket, which is drained at the specified rate. If too many cells arrive at once, the bucket may overflow. The overflowing cells are called non-conforming and may or may not be admitted in to the network. If admitted, the cell loss priority (CLP), bit of the non-confirming cells may be set so that they will be first to be dropped in case of the overload [5].

The diagram in the figure 1 below illustrate how this algorithm works The GCRA depends on two parameters: increment I and limit L (GCRA(I,L)). I characterize the drain rate of the bucket and L characterizes the height of the bucket. The greater the height of the height of the bucket, the more the cells the bucket can buffer.

If the cells are pouring too quickly into the bucket, the bucket will overflow and cells will be lost. In the flowchart above, TAT means Theoretical Arrival Time and $t_a(k)$ refers to the arrival time of a cell. According to the ATM Forum, it is necessary to police the PCR, using I = 1/PCR and L= CDV as GCRA parameters.

4.2 Explicit Rate-Based Scheme

Based on the type of the traffic and the quality of service desired, ATM application can use one of the service categories described under section 2. Of these ABR is the most commonly used service category. It allows ATM network to control the rates at which delay-insensitive data sources may transmit. ABR traffic management can be fairly divided into two approaches: credit-based and rate-based.

The credit-based approach uses per-hop per-VC window flow control, while the rate-based approach which performs better uses end-to-end rate based control. Although ATM Forum traffic management version 4.0 specifications allows older Explicit Forward Congestion Indicator (EFCI) switches with binary feedback for backward compatibility, the suggested Explicit Rate Indicator for Congestion Avoidance (ERICA) switch algorithm in this work provide better performance and faster control.

4.3 ERICA Switch Algorithm and Principle

Target cell rate = Target utilization x Link capacity
Target Utilization = *fn*(Current load, Queue length, Queue drain time goal)

- Input rate (and not queue length) is the load measure.
- Congestion avoidance (and not congestion control) should be the goal.
- Transient performance (and not the steady state performance) is more important.

This algorithm shows to be efficient, fair, fast transient response, being implemented by several vendors, able to handle bursty TCP traffic. It allows low delay even at 100% utilization and provides stability in the presence of high frequency VBR background traffic.

5. CONCLUSION

Traffic management is a key to success of ATM. It functions to prevent and control congestion across ATM networks and provide the quality of service (QOS) required. Due to larger bandwidth distance product, the amount of data lost due to simultaneous arrivals of burst from multiple sources can be larger. For the success of ATM, it is important that it provides a good traffic management for both bursty and non-bursty sources. Based on the type of the traffic and the quality of service desired, ATM application can use one of the five service categories. CBR,rt-VBR, UBR, and ABR. Of these ABR is the most commonly used service category. It allows ATM network to control the rates at which delay-insensitive data sources may transmit. Thus, the link bandwidth not used by CBR and VBR applications can be fairly divided among ABR sources.

Currently, we are working on the implementation of the proposed architecture, but this work can be improved upon in several ways, especially for the case of multiple classes. The system should be tested with other traffic models that can mimic audio and image files, as well with different ATM network topologies.

REFERENCES

[1] Allyn, R (1994). Packet Discard Strategies for Controlling ATM Congestion, ATM Forum Traffic Management Sub-working Group submission.

[2] Amir, A. and Hui, J., "A Rate-Based Feedback Traffic Controller for ATM Networks", IEEE ICC 94, New Orleans, pp 166)5-1615,1994

[3] Aranuwa, F.O. (2010). Traffic Control and Bandwidth Allocation in ATM Networks. Conference Paper at Adekunle Ajasin University, Akungba – Akoko, 2010.

[4] Barnhart A.W. (1994). "Explicit Rate Performance Evaluation," AF-TM 94-0983r1, October 1994.

[5] Boyer, P.E. and Tranchier, D.P. (1992). "A Reservation Principle with Applications to the ATM Traffic Control, Computer Networks and ISDN Systems, Vol.24,1992,pp.321-334.

[6] Charny, A. (1994). "An Algorithm for rate Allocation in a Cell-Switching Network with Feedback", MIT TR-601, May 1994.

[7] Francesco, B., Pantelis, L. and Vasillios, D. (1999). "ATM Connection Admission Control pRAM based Artificial Neural Networks", University of Pisa (Italy), at King's College London sponsored by the EU SOCRATES exchange programme.

[8] Jain, R. (1990). "Congestion Control in Computer Networks: Issues and Trends," IEEE Network Magazine, May 1990, pp. 24-30.

[9] Jain, R. (1992). "A Delay-Based Approach for Congestion Avoidance in Interconnected Heterogeneous Computer Networks," Computer Communications Review, Vol.19, No 5, October, 1989, pp.56-71.

[10] Newman, P. (1994). "Traffic Management for ATM Local Area Networks" IEEE Communications Magazine. August 1994, pp.44-50.

[11] Roberts, L. (1994). " The Benefits of Rate-Based Flow Control for ABR Service, "AF-TM 94-0796, September, 1994.

[12] Siu, K. and Jain, R. (1995). A Brief Overview of ATM: Protocol layers, LAN Emulation, and Traffic Management. Computer Communication Review (ACMSIGCOMM).

[13] Sathaye, S. (1994). " Draft ATM Forum Traffic Management Specification Version 4.0," AF-TM-95-0013, December 18, 1994.

[14] Yao-Ching, L and Douligeris C. (2000). "Feedback Congestion Controller for ATM Networks Using a Neural Network Traffic Predictor. University of Mianmi, Coral Gables

Embedded Computer-Based Lecture Attendance Management System

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ABSTRACT
Electronic cards like magnetic cards and smart cards have been used worldwide for different functions such as electronic payment system (credit card and debit/ATM cards), electronic voting system, personnel identification system and security system. In this paper, we present an electronic card-based solution to the lecture attendance problem in higher institutions in the developing countries. Ours is based on single-chip computer based subsystems interfaced serially to the serial port of the digital computer. The developed system could speed up the process of taking students lecture attendance and allows for error free and faster verification process of authenticating student lecture attendance policy required for writing examination in a campus environment.

Keywords: Microcontroller, PIC16f84, Lecture, Attendance, AT89C52, Serial Port

1. INTRODUCTION

In most institutions of higher learning in the developing countries, no student is qualified to write examination unless a record of minimum of seventy percent of the lecture attendance is attained. This policy has not been totally observed because a proper protocol of observance has not been established.

The usual practice is that students are given sheets of paper to write down their names, matriculation number and signature. This manual method of taking attendance is obviously not effective as it is attributed to the following challenges: The sheets of paper become cumbersome and untidy as the population of student increases; time consuming and a waste of human and material resources; high level of impersonation as absentee can be on the list through their friends that attended the class due to the lower lecturer/student ratio and large class size. Consequently, it is very difficult to manage the attendance and determine whether each student actually made seventy percent (70%) of lecture attendance.

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As a result of these flaws in the classical method of taking student attendance, there is need for faster, easier, more accurate and effective method, using modern technology of the present age. A number of tools have been used to solve this problem, this include Barcode Readers [10],Radio Frequency Identification System[15] and Bluetooth[16].These tools were not only expensive when first introduced, they had limited usage[13].

This work seeks to shift paradigm from these referred methods by formulating and implementing a simplified and cost effective model of embedded computer based solution to the classical and/or manual method of managing student lecture attendance problem in higher institutions in developing countries like Nigeria. The paper is divided into seven sections: section 2 discusses related works in the problem domain, Section 3 highlights the general overview of the proposed system, Section 4 details design considerations of the system, both at the hardware and software level, Section 5 discusses the operation and how the system was tested in conformity to system design and functional objectives. Section 6 concludes the paper while section 7 identified gaps and make recommendations for future improvement.

2. RELATED WORKS

A number of related works exist in literature on application of different electronic engineering principles to student attendance monitoring problem. In [2], an automatic attendance system using fingerprint verification technique was proposed. The fingerprint technique verification was achieved using extraction of abnormal point on the ridge of user's fingerprint or minutiae technique.

The verification confirms the authenticity of an authorized user by performing one to one comparison of a captured fingerprint templates against the stored templates in the database. The proposed automatic attendance system signals either true or false based on logical result of previous one to one verification of person's authenticity. Authors in [6] also reviewed and proposed biometric system using fingerprint identification for attendance automation of employees in an organization.

Consequently, authors in [14] proposed student wolf pack club tracking system to simplify and speed up the process of student wolf pack club ticket distribution for athletic event. Similar solution was proffered for tracking and counting students in [13] during Eastern Mediterranean University seminars using barcodes and readers. Also, authors in [11] proposed the use of electronic finger print scanner to solve students lecture attendance monitoring problem of Bells University of Technology, Ota, Nigeria.

The fingerprint technique verification was achieved using extraction of the biometric fingerprint feature of each undergraduate student. The application software of the proposed system lacks report generation and audit trail system and thus made students attendance to be entered manually. In [9] authors proposed student tracking using Radio frequency identification system (RFID). It involves the use of the student card to get student attendance. The author tried to solve the problem of manual computation of attendance but his work does not eliminate the risk of impersonation. Similar solution to attendance monitoring problem can be found in barcode readers as does in [13].

In [2], Artificial Neural Networks and Facial Recognition in Artificial Intelligence were used to develop a security door system where authorization of facial appearance of privilege users in the database is the only guarantee for entrance. In the system, the personal computer processes the user's face recognized by the system digital camera and compares data with privileged users in the database. The control program either sends a control signal to open the electromechanical door upon facial existence or deny entry.

Ours is a simplified and cost effective model of embedded computer based automated students lecture attendance system that allows lecturers to electronically monitor student attendance and verify if each student made the required percentage to sit for an examination using an improvised electronic card. The proposed system does not only speeds up the process of taking attendance but allows for less error and faster verification process of authenticating student lecture attendance policy required for writing examination in a campus environment.

3. SYSTEM OVERVIEW

The proposed system provides solution to lecture attendance problem through coordinated hardware and software design synergy that exists between an improvised electronic card and the card reader serially interfaced to the digital computer system [9]. The electronic card is a model of a smart card containing the student identity (ID-Name, Matriculation Number and five pin encrypted code).

The student ID is authenticated by the card reader which compares the entrance code with the encrypted code on the card swiped through the card reader. The student is granted and/or denies specific lecture attendance based on the result of the comparison by the backend software system running on the PC to which the card reader is serially interfaced as shown in Figure 1.0

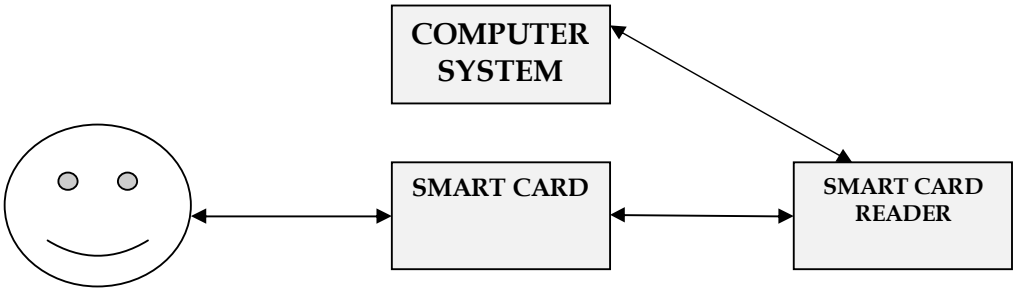

Figure 1.0: Block diagram of an Embedded Computer Based Lecture attendance system

4.0 SYSTEM DESIGN

In an attempt to solve above the following lecture attendance problem, the proposed system from figure 1.0 interacts with students on lecture by lecture basis for proper student identification, organization and authentication. The system major design considerations were functionality, simplicity, availability of component, ease of use and cost. From the block diagram, the electronic smart card contains an embedded computer based system or microcontroller with a non-volatile storage memory system to hold student identification details.

The card reader also contains a microcontroller which receives the data and sends data to the computer system for attendance authentication and/or denial. The computer system contains an interactive Object Oriented paradigm (OOP) based software system that modifies student attendance information and updates it on the system database. It also provides an interface where attendance is taken, and results could be given when required. The section 4.1 and 4.2 give the detail hardware and software design considerations for the proposed system design idealization.

4.1 HARDWARE DESIGN CONSIDERATIONS

The hardware subsystem consists of two main parts the card and the card-reader. These parts are discussed as follows:

4.1.1 The Electronic Smart Card

The card initial design considerations include data storage and data security. For data storage, different chips were considered, they include: serial EEPROM, RAM, Battery Backed-Up RAM, and SD memory cards. For cost consideration, an intelligent microcontroller device that will not only provide data security but also has the ability for permanent storage was chosen. Although there are different options of microcontrollers such as; PIC16f648a which has large memory capacity and operates at high speed and have a lot of additional features, but they were not readily available and expensive. The microcontroller used for the card is the PIC16F84A, which is readily available and easy to use.

The PIC16F84A belongs to the mid-range family of the PICmicro® microcontroller devices. Figure 2.0 shows the block diagram of the device. The program memory contains 1K words, which translates to 1024 instructions, since each 14-bit program memory word is the same width as each device instruction. The data memory (RAM) contains 68 bytes and Data EEPROM is 64 bytes. There are also 13 input/output (I/O) pins that are user-configured on a pin-to-pin basis [1]. Some of the pins are multiplexed with other device functions.

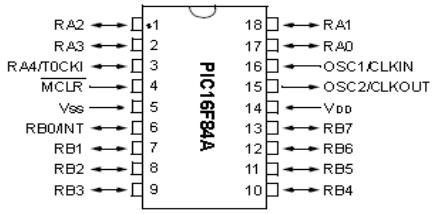

Figure 2.0: PIC16F84 pin details

For the card microcontroller oscillation design consideration, the data sheet in [7] of the PIC16F84 stipulated that the crystal oscillator can operate in four modes: 1) LP Low Power Crystal 2) XT Crystal/Resonator 3) HS High Speed Crystal/Resonator and 4) RC Resistor/Capacitor. Our card design emphasize the XT mode (crystal/resonator) shown in figure 3.0.

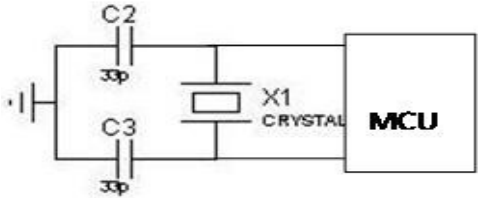

Figure 3.0: Crystal Resonator XT Configuration

A crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation. This is illustrated in Table 1.0.

TABLE 1.0: Capacitor Selection for Ceramic Resonators

Mode	Freq	OSC1/C1	OSC2/C2
XT	455 kHz 2.0 MHz 4.0 MHz	47 - 100 pF 15 - 33 pF 15 - 33 pF	47 - 100 pF 15 - 33 pF 15 - 33 pF

From the table above, a 4.5MHZ crystal oscillator with two 33pf capacitors attached, constantly supply power irrespective of the break in contact with the reader. Higher capacitance increases the stability of the crystal oscillator while lower capacitance reduces start-up time. Any size of crystal oscillator could have been used, because the higher the crystal oscillator, the more power it consumes and the lower it is, the more time it would take for the card to transfer data to the card reader so, 4.5MHZ was a good compromise between power consumption and speed.

The processing speed of the PIC18F64 from the data sheet [7] is:

PIC18F64 processing speed = Frequency of Crystal Oscillator/4 = 4.5/4=1.15MHz.. (1)

So, the processing speed of the PIC18F64 Microcontroller on the card is 1.15MH. The overall circuit diagram for the system electronic card subsystem is thus shown in figure 4.0:

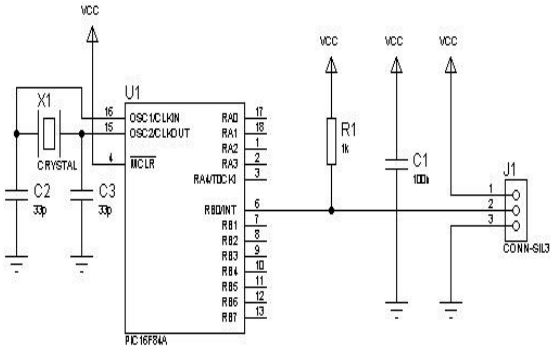

Figure 4.0: Electronic card circuit diagram

For cost and space design reasons, different options were considered for the integration of the various electronic components attached to the individual subsystems. Two methods under consideration were to use a veroboard or try to design a printed circuit board (PCB) to attach the microcontroller of the card and card reader. To ensure high precision when sliding the electronic card through the reader and minimize error in system operation, our improvised lecture entrance electronic card features the design of 2.2 inches X 3 Inches PCB in single sided copper clad of one (1) oz of figure 4.0 as figure 4.1.

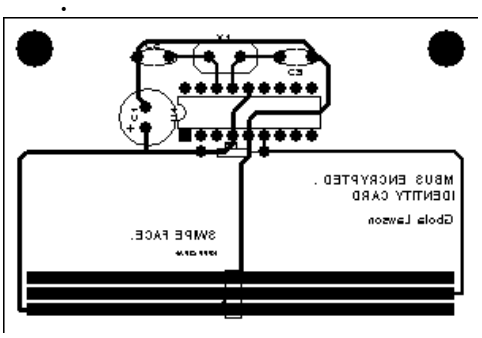

Figure 4.1 PCB Layout for card

4.1.2 The Card Reader

The size and simplicity of the device were the two major design considerations taken the in card reader design. Its primary functions are as follows: 1) Ability to read from and write to the improvised lecture entrance card in a secure manner, 2) Ability to communicate with the computer system and effectively interacts with each student upon arrival to lecture venue.

For the communication with card, the microcontroller used for the card reader was the Atmel's AT89C52 which is a variation of Intel's 8051 (with similar instruction sets). AT89C52 is readily available in the open market and has a low-power, high-performance CMOS 8-bit microprocessor with 256 bytes of data RAM, 8K bytes of Flash programmable and erasable read only memory (EEPROM). Other features of the AT89C52 MCU considered for this application are: 32 Programmable I/O Lines; Eight Interrupt Sources; Endurance: 1,000 Write/Erase Cycles; Fully Static Operation: 0 Hz to 24 MHz, Three-level Program Memory Lock and Low-power Idle and Power-down Modes. The embedded data RAM acts as a temporary storage or buffer for transferring data between the computer system and the card. AT89C52 MCU is volatile and would only retain data while power is connected to the device.

Consequently for oscillation design consideration, the crystal oscillator used was faster than that on the card. The MCU operates at 1/12 of the crystal oscillator speed (compared to the ¼ of the PIC18F64). A higher frequency that would be in the same range with the processing speed of the card is needed. The processing speed of the AT89C52 which from the data sheet from equation 1, thus is:

AT89C52 processing speed = Frequency of Crystal Oscillator/12=8/12=0.66MHz (2)

The recommended capacitance for the capacitor according to the data sheet for the crystal oscillator was C1, C2 = 30 pF, 10 pF for crystals respectively. Since 33pf capacitor was used for the entrance electronic card we decided to use the same for the card reader's crystal oscillator. There is also a power on reset circuit (Figure **5.0**) connected to the pin 9 (RST) of the AT89C52 MCU. When power is connected to the device, current flows through the capacitor (c) to the RST pin for a time (t) till the capacitor becomes fully charged, since the RST pin is active high, the voltage present at the pin causes the MCU to reset, after which the capacitor becomes cut off and the pin is connected to the ground through resistor (R).The time it takes to reset the MCU is: $0.5 = e^{-t/RC}$. Thus, t was calculated as: t = log 0.5 X (-RC) =t = log 0.5 X (-5600 x 10E-6) t = 1.6858×10^{-10}sec (3)

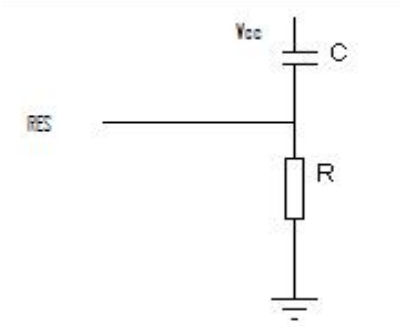

Figure 5.0: The Reset Circuit

A red light emitting diode (LED) was connected to pin 21 of the MCU. Its serves as an indicator to show when the card is connected to the reader (The led comes on) and it blinks when data has been stored into the card. The 1k resistor (R2) connected to the LED acts as a limiting resistor to reduce the voltage across the diode. Pin 32(port 0 pin 7) was used for simplex communication with the card. For communication with computer system, we considered serial interfacing with the computer system, this was also a criterion we used in selecting the MCU used for the reader since AT89C52 MCU has programmable serial channel capabilities which enables it to serially transmit and receive from the computer.

In the chip, Pin P3.0/ RXD was used to receive data while Pin P3.1/ TXD was used for data transmission. UART chip takes the parallel output from processor bus and transform it to serial form for transmission and vice versa [5]. Typical chip along this purpose is MAX232 Transceiver. Because, the 5v (0 – 5v used) in the devices was incompatible with the 25v (-12v to + 12v) signal level used by the serial port. A MAX232 transceiver was introduced to interface the reader and the computer system. The MAX232E line drivers/receivers are designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±15kV, electrostatic discharge (ESD) shocks, without latch up.

Other power electronic components used for the design include: KA7805 Voltage Regulator and Adjustable base voltage and current capacitors. For durability, flexibility and power protection of the overall electronic circuitry; it was necessary for the reader to operate over a wide range of voltage. This was achieved by introducing a voltage regulator KA7805 IC. The IC is part of the KA78XXA series of three-terminal positive regulator with several fixed output voltages. KA7805 has a fixed output voltage of (5Vdc), with a wide range of input voltage between 3.5Vdc to 6Vdc, it employs an internal current limiting, thermal shut down and safe operating protection, making it essentially indestructible[8].

If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents. The two 10uf capacitors C1 and C2 in figure 6.0 connected to the voltage regulator are used to regulate the flow of current. In our design, the KA7805 acts as a constant voltage (5v) power source for both the reader and the card when connected [6]. The overall circuit diagram for the card reader is shown in figure 7.0:

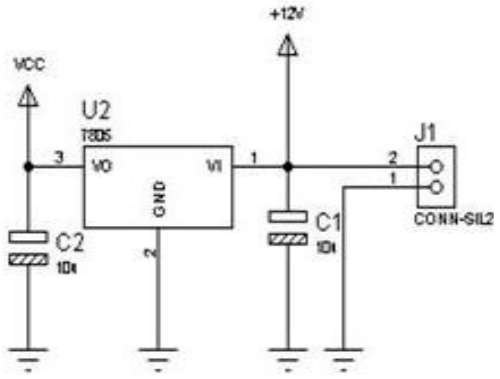

Figure 6.0: Three Terminal 7805 circuit for power protection

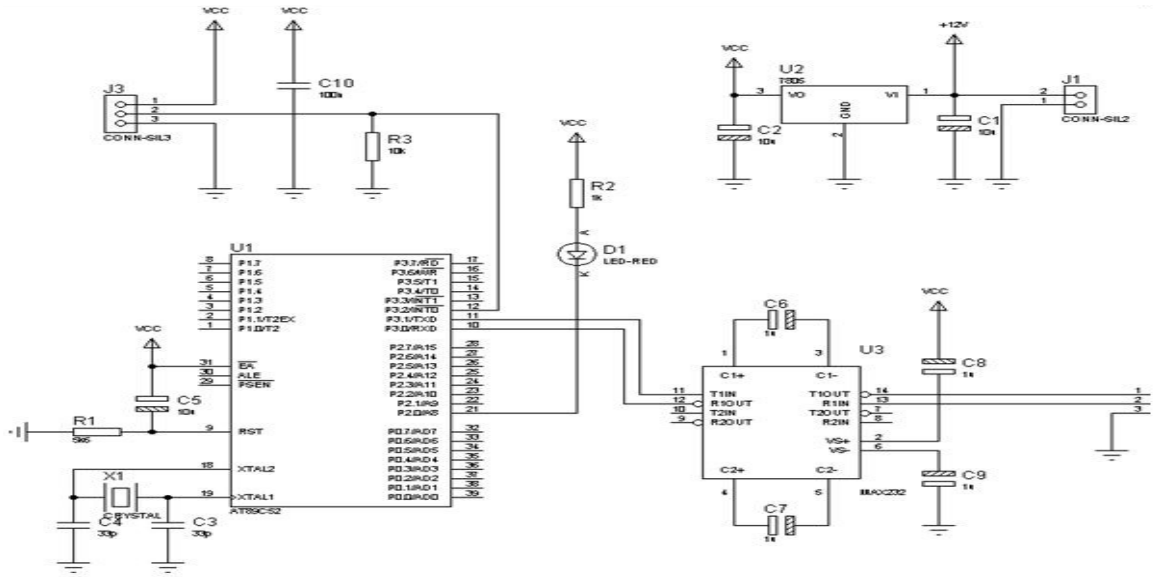

Figure 7.0: Card reader overall circuit diagram

Consequently for the reader, the card reader features the design of 3.6 inches X 5.4 Inches PCB in single sided copper clad of one (1) oz of figure 7.0 as figure 7.1. Also noted was the swiping space of the reader because of the electronic card 1.2mm thickness.

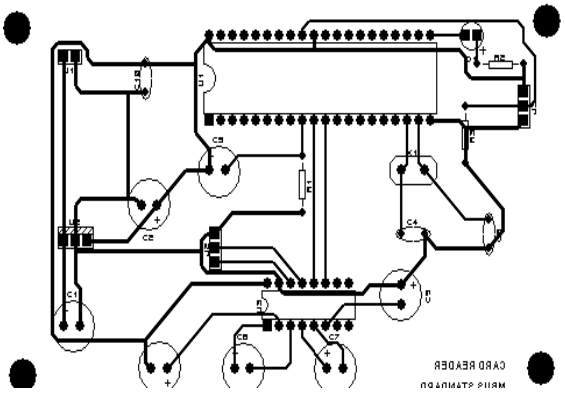

Figure 4.1 PCB Layout of the Card reader

4.2 SOFTWARE DESIGN CONSIDERATIONS

The software design was considered in two schools of thought: embedded microcontroller development and OOP Software based system development.

Embedded Microcontroller Development

5.0 SYSTEM OPERATION, TESTING AND

The microcontroller programs can be written in C, Max-Forth or Assembly. The small procedural paradigm C programming language was chosen for flexibility and code economy reasons. Program codes could be reused in C Programming, and allowed excellent flexibility in future modification.

For the lecture entrance card, we used HITECH MPLAB software, which provided us with a series of tools such as the PIC LITE compiler, an emulator interface and linker in programming the PIC16F84 microcontroller. The PIC PROG programmer was used to burn the code into the PIC16F84.For the reader, the programming language platform used to program the AT89C52 microcontroller was the KEIL C compiler, while ISP in circuit programmer was used to burn the code into the microcontroller.

OOP Based Software System Development

The software system is architecturally, a two tier client server software system. The system front end or the user interface was design and implemented with Visual BASIC 6.0 (VB6), a rapid development (RAD) tool that allows application development in less time. The main reason why VB6 was considered for the system graphical user interface (GUI), is that, it contains software methods that allow easy access to the serial communication port of the computer. The backend was implemented with MySQL 2000 DBMS for robustness and scalability reasons for database development.

DISCUSSION

The entire system operates by swiping the improvised electronic card along the edge of the card reader. The swipe mechanism was used in contrast to an insert mechanism due to easier implementation and communication of the card with the reader. On the card are 0.18 inches, three parallel conducting lines, two for power (+5vdc and ground) and one in the middle for half duplex communication with reader. The reader has three parallel conducting springs corresponding to each conducting line of the card, in four different points to ensure that adequate contact is made between the card and reader. By swiping the card on the reader ,the automated lecture attendance management software system graphical user interfaces show as follows for student to register attendance:

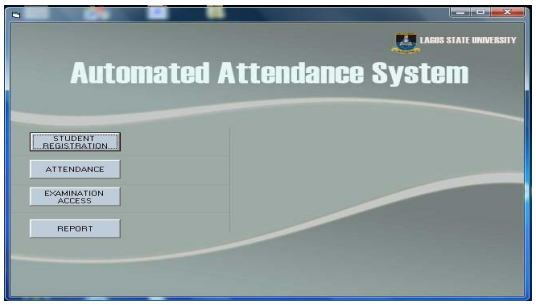

Figure 8.0: Home Page

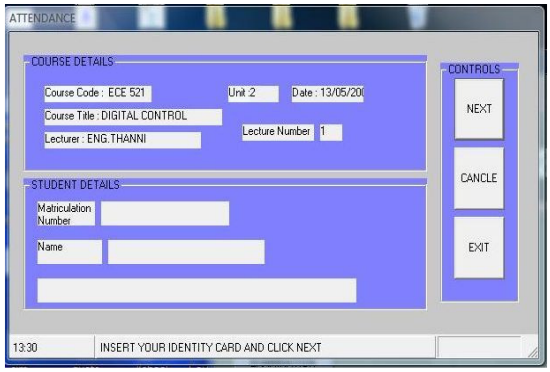

Figure 9.0 Interface for logging attendance

The application was developed to automatically detect when the card is slot into the reader (through the serial port) and proper pre-configuration of the card. The system requests for the student PIN and automatically increments the student's attendance per course at the backend (The database) as shown in Figure 8.0 and Figure 9.0.

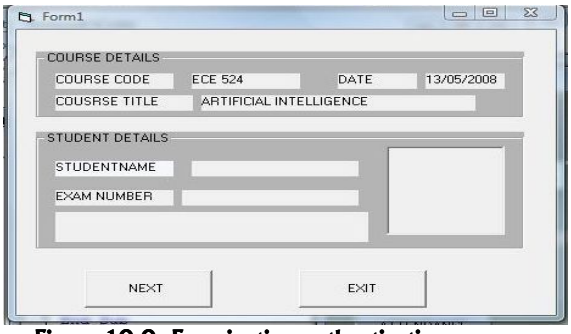

Figure 10.0: Examination authentication

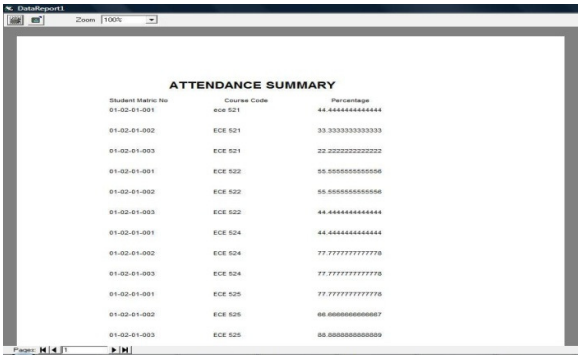

Figure 11.0 Report of Student attendance

Figure 10.0 used shows the GUI for examination authentication. Similar to the attendance form, it detects the card and displays what percentage per lecture each student has attended compared to the number of lectures taken by the lecturer. If 70% and above lecture attendance record is made by the student, it displayed that the student is qualified to write the examination. Consequently, Figure 11.0 is a printable sheet that displays the percentage of lectures attended by student for various courses for official verification.

During system testing, it was discovered that the card reader could not detect electronic entrance card, when inserted, so we used R1 (figure 4.1) as a pull up resistor to represent a signal alert to the reader when entrance card is swiped against it as shown in figure 4.0. The card reader and lecture attendance electronic card was package with synthetic materials to protect the component from mechanical damage, extreme heat, humidity and temperature variation as shown in figure 12.0, 13.0 and figure 14.0 respectively.

Table 4.1 speed of manual attendance compared to electronic method of attendance (sample for 25 student

Student number	Manual Attendance in (sec)	Automated Lecture Attendance in (sec)	Automated Exam Attendance in (sec)
1	14.97	6.02	4.01
2	15.16	6.07	4.01
3	15.18	7.05	4.01
4	16.54	7.07	4.03
5	16.59	7.12	4.05
6	16.92	7.14	4.05
7	16.95	7.26	4.05
8	17.61	7.54	4.06
9	17.72	7.55	4.57
10	17.78	8.02	4.57
11	18.01	8.05	4.62
12	18.25	8.13	4.7
13	18.62	8.24	4.7
14	19.19	8.45	4.85
15	19.34	8.52	4.93
16	19.67	8.55	5.06
17	19.72	8.62	5.12
18	19.85	8.72	5.13
19	19.89	9.45	5.27
20	20.52	9.55	5.31
21	20.91	10.05	5.47
22	22.03	10.12	5.65
23	23.16	10.14	5.77
24	23.19	11.52	5.77
25	24.21	11.64	5.99

Figure 12.0: Electronic Card

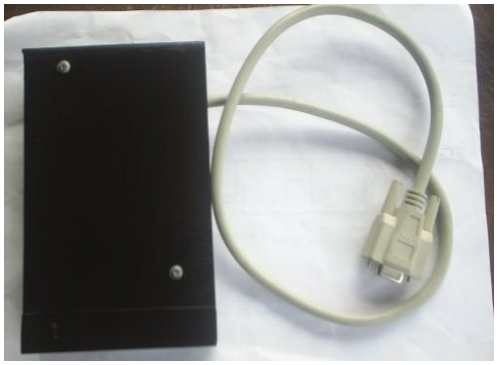

Figure 13.0: Connections for The System

Figure 14.0: Left and Top view of the Card reader

The effectiveness of our system software and hardware design consideration was further tested by comparison of time difference in the conventional/manual method of lecture attendance with the proposed electronic method by testing the system with twenty five students of the Department of Electronic and Computer Engineering, Lagos State University, Epe, Nigeria. The study from table 2.0 shows that the electronic approach was more accurate, faster and efficient.

6.0 CONCLUSION

This paper has successfully presented a simplified, low cost embedded computer based system solution to the management of lecture attendance problem in developing countries. The operation of the system is based on guidelines surrounding the conduct of lecture on one (the Lecturer) to many (students) lecture environment and policy of taking and writing examination in campus environment. The system could authenticate, verify, grant and/ or deny a student attendance to lecture when an electronic card is swipe on the card reader. PIC serves as a Microcontroller unit(MCU) for vehicle of data storage while different programming language platforms considered are fundamental to software design based on the initial requirements gathering, specifications, and planned operation of the system. The major strength of the system lies in its portability and high scalability but with less flexibility in programming as compared to the previous design and implementation in [3, 4, 6, and 12]. By careful examination, it can be inferred that the proposed system could not only speed up the process of taking attendance but allows for less error and faster verification process of authenticating student lecture attendance policy required for writing examination in a campus environment.

7.0 RECOMMENDATION FOR FUTURE WORK

The functionalities of the system can be further enhanced through the following recommendations:

- The linkage of the proposed automated system at each lecture venue to a dedicated server centrally managed by the University ICT Department. This would allow the system to extract user information from the ICT database directly and eliminate the need to store this information within the card and increase the overall system response time.
- Investigate student attendance monitoring through hybridized Biometric features like face, iris fingerprint and Wireless radio transmission through RFID for better performance.

REFERENCES

[1] Arulogun O.T, Fakolujo O.A, Olaniyi O.M, Fenwa D.O, Olaniyan A.B (2010): "Design of Embedded Computer Based Household Electricity Power Management System", Proceedings of the First International Conference on Engineering and Technology Research, 28th -30th September, 2010, Lautech Ogbomoso, Oyo State,Nigeria.

[2]Arulogun O.T, Omidiora, O., M. Olaniyi, and A.A. Ipadeola (2008), "Development of Security System Using Facial Recognition", Pacific Journal of Science and Technology, 9(2):377-386.

[3]Chitresh, S and Amit K(2010),"An efficient Automatic Attendance Using Fingerprint Verification Technique ",International Journal on Computer Science and Engineering (IJCSE),Vol. 2 No. 2,pp 264-269.

[4] Henry. S, S. Arivazhagan and L. Ganesan, (2003), "Fingerprint Verification Using Wavelet Transform", International Conference on Computational Intelligence and Multimedia Applications, 2003.

[5] Jeff T. (2008), "Serial Port Howstuffworks", Available online at Http://computer.howstuffworks.com/serial-port1.htm, Retrieved 15th June 2008.

[6] Maltoni D, D. Maio, A. K. Jain, S. Prabhaker (2003), "Handbook of Fingerprint Recognition", Springer, New York,Pp 13-20.

[7]Microchip Inc. (2003),"PIC16F84 Data Sheet for 28/40/44 Enhanced flash Microcontrollers", USA

[8] Lawson A (2008),"Design and Construction of an automated attendance system using Electronic Card",B.Sc Dissertation, Lagos State University: Epe, Nigeria.

[9] Mahyidin M. (2008), Student Attendance Using RFID System ,B.Eng Thesis, Electrical and Electronics Engineering Department, University of Malaysia Pahang, Retrieved online at http://umpir.ump.edu.my/345/1/3275Firdaus.pdf on 21st September,2011.

[10] Shoewu, O. and O.T. Baruwa. 2006. "Design of a Microprocessor Based Automatic Gate", Pacific Journal of Science and Technology, 7(1):31-44.

[11] Sriram, T. , Vishwanatha Rao, K., Biswas, S., Ahmed, B., (1996),Applications of Barcode Technology in Automated Storage and Retrieval systems, Industrial Electronics, Control, and Instrumentation, Proceedings of the 1996 IEEE IECON 22nd International Conference, Taipei Taiwan, Volume 1, Page(s) 641 – 646,5-10

[12] Kokumo B (2010), Lecture Attendance System Using Fingerprint, B Tech Dissertation, Bells University of Technology,Ota,Nigeria.

[13] Kizildag M, Basar E,Celikag M, Atasoylu E and Mousavi S(2007),"An Automated Attendance Monitoring and Registration System for EMU's SPIKE Seminar series", Retrieved online at http:// http://init.org.pk/papersandpublications/Paper21.pdf on 26th September,2011.

[14]Victor S, Jonathan M, Reece J, and Lemire J (2003),"Student Wolf Pack Club Tracking System", North Carolina State University. USA.

[15] Weinstein, R (2005), RFID: a technical overview and its application to the enterprise, IT Professional, Volume 7, Issue 3, Pp27 – 33.

[16][B]http://www.bluetooth.org, "The Official Bluetooth Membership Site", Last Visited 20th Septemebr 2011.

Constructing Ontologies In Owl Using Protégé 4

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ABSTRACT
In the light of improving the World Wide Web, researchers are working towards the Semantic Web, a Web of information that machines can understand and process Ontologies and ontology-based applications are its basic ingredients. Protégé is an ontology development tool and knowledge-acquisition environment developed by Stanford Medical Informatics. It has a graphical user interface which enables ontology developers to concentrate on conceptual modeling without knowing or thinking about syntax of an output language. Protégé has a flexible knowledge model and extensible plug-in architecture. This paper describes how Protégé-4 can be used for constructing ontologies in OWL. We were able to establish that an ontology building process is the basis for application development. It will start with the brief description of semantic web, ontology and ontology languages.

Keywords: Semantic Web, Ontologies, Protégé, design methodologies, OWL

1. INTRODUCTION

In the light of improving the World Wide Web, researchers have found enormous amount of information and knowledge. An emerging problem of significant importance is the efficient retrieval and reuses these resources. A promising approach proposed by Tim Berners-Lee is the reformation of the Web, as it exists, into the "Semantic Web". As Berners-Lee says "The Semantic Web is an extension of the current Web in which information is given well-defined meaning [1]". It is the idea of having data on the Web defined and linked in a way that it can be used for more effective discovery, automation, integration, and reuse across various applications.

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Ontologies are becoming the corner stone of the Semantic Web (SW). Ontologies aim at capturing domain knowledge in a generic way and provide a commonly agreed understanding of a domain. They are shared conceptualizations of a domain, and they possibly include the representations of these conceptualizations [2]. Ontologies are independent from the applications that use them. This leads to easier software and knowledge maintenance, and contributes to the semantic interoperability between applications [3].

Among the representation formalisms for ontologies, the Web Ontology Language (OWL) is the widely accepted standard for representing and sharing knowledge in the Semantic Web context.
The OWL language is divided into three syntax classes:

- OWL-Lite - classification hierarchy and simple constraints
- OWL-DL - maximum expressiveness with desirable computational properties for reasoning.
- OWL-Full - maximum expressiveness and syntactic freedom of RDF with no computational guarantees.

Particularly, OWL-Lite and OWL-DL belong to the description logics [4]. From the existing tools (e.g. WebOnto, OntoEdit), Protege-4 is chosen for implementation because it enables the construction of domain ontologies, customized data entry forms to enter data. Protégé allows the definition of entities, classes, class hierarchies, object properties, data properties, and individuals [16].
This paper focuses on how Protégé-4 can be used for constructing ontologies in OWL. The approach is illustrated through simple examples of creating ontology.

2. RELATED WORKS

The pepper ontology project is not the first to aim at building ontology in the context of knowledge acquisition and management for an enterprise or researcher. Related efforts are knowledge management project like the TOVE-project [19], and the Enterprise Ontology [20].

Both TOVE and the Enterprise Ontology (EO) aim at modeling a complete enterprise. They do this with a number of ontologies which together form a complex framework. A brief analysis showed that TOVE and Enterprise ontology contain many concepts that would not be needed for the pepper ontology, and that it would be very difficult to only reuse the needed concepts because they depend on other concepts. Thus, the idea of reusing either TOVE or EO was abandoned.

3. PROTÉGÉ-4

Protégé is an ontology and knowledge base editor produced by Stanford University. Protégé is a tool that enables the construction of domain ontologies, customized data entry forms to enter data. Protégé allows the definition of classes, class hierarchies, variables, variable-value restrictions, and the relationships between classes and the properties of these relationships. Protégé is free and can be downloaded from http://protégé.stanford.edu. Protégé comes with visualization packages such as OntoGraph, OWL Viz, etc.; all of these help the user visualize ontologies with the help of diagrams. Stanford University is doing a magnificent job of continually improving Protégé.

As part of its last update, Protégé now includes an interface for SWRL (Semantic Web Rule Language), which sits on top of OWL to do math, temporal reasoning, and adds Prolog-type reasoning rules. Stanford has a tutorial that covers the basics of using Protégé with the OWL plug-in. Additional support can be obtained by consulting others on the Protégé/OWL news group.

The main strong point of Protégé is that it supports at the same time tool builders, knowledge engineers and domain specialists. This is the main difference with existing tools, which are typically targeted at the knowledge engineer and lack flexibility for meta-modelling. This latter feature makes it easier to adapt Protégé to new requirements and/or changes in the model structure.

4. ONTOLOGY DEVELOPMENT

We describe an iterative approach to ontology development: We started the ontology development with collecting requirements for the envisaged ontology. By nature this task is performed by a team of experts for the domain accompanied by experts for modeling. The outcome of this phase is a document that contains all relevant requirement specifications (domain and goal of the ontology, design guidelines, available knowledge sources, potential users and use cases and applications supported by the ontology). A semi-formal ontology description is extracted from the requirement specification document, i.e. a graph of named nodes and directed edges, both of which may be linked with further descriptive text.

To implement a methodology it is desirable to have a tool that reflects and supports all steps of the methodology and guides users step by step through the ontology engineering process. Along with the development of the methodology we therefore extended the core functionalities of Protégé. First, we would like to emphasize some fundamental rules in ontology design to which we will refer many times. These rules may seem rather dogmatic. They can help, however, to make design decisions in many cases. Ontology is typically built in more-or-less the following manner:

1. **Acquire domain knowledge:**
   Assemble appropriate information resources, their characteristics and the terms to describe things in the domain of interest. The output is a natural-language ontology specification document.
2. **Organize the ontology:**
   Domain terms are identified as entities, classes, individuals, data properties or object properties and each are represented using an applicable informal representation.
3. **Flesh out the ontology:**
   Add concepts, relations, and individuals to the level of detail necessary to satisfy the purposes of the ontology.

4. **Check and classify your work:**
   Reconcile syntactic, logical, and semantic inconsistencies among the ontology elements. Consistency checking may also involve automatic classification that defines new concepts based on individual properties and class relationships.
5. **Commit the ontology:**
   Verification of the ontology by domain experts.

5. METHODOLOGY FOR ONTOLOGY CONSTRUCTION

At present the construction of ontologies is very much an art rather than a science [6].This situation needs to be changed, and will be changed only through an understanding of how to go about constructing ontologies. In short what is needed is a good methodology for developing ontologies. This attempt to formalize the ad-hoc process consists of the following steps [7]

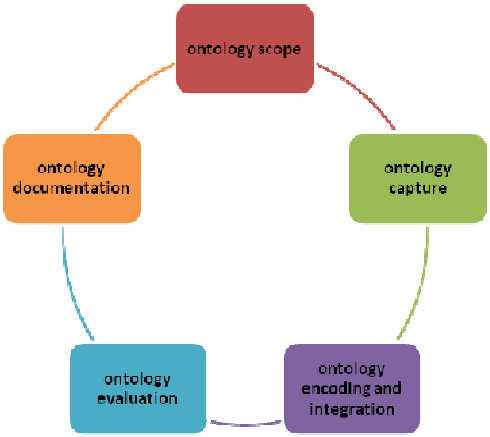


Fig1. Ontology Construction Methodology

Scope
Identify the range of intended users, determine the purpose of the ontology, and identify user requirements for systems using ontology.

Capture
Identify key concepts and relationships in the domain of interest, produce precise definitions for such concepts and relationships.

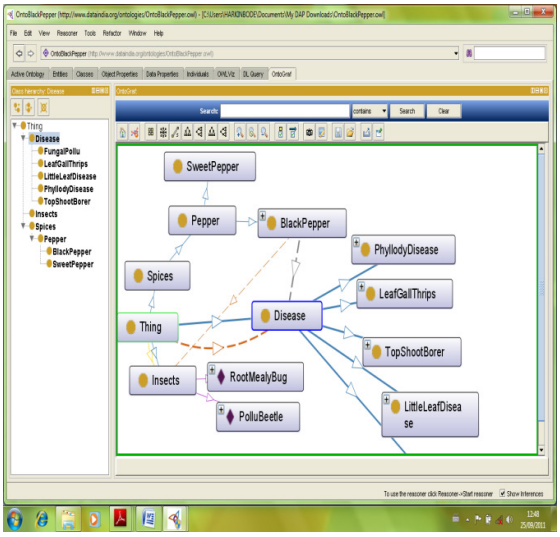
Encoding and Integration
Committing to the basic terms that will be used to specify the ontology, choose representation language and coding the ontology. Ontology integration deals with associating key concepts and terms in the ontology with concepts and terms of other ontologies; that is, incorporating concepts and terms from other domains.

Evaluation
Checking on competency questions (CQ).Ontology must be able to answer all the given CQ.

Documentation
Effective knowledge sharing requires adequate documentation, all assumptions should be documented.

6. A SIMPLE ONTOLOGY
Look at the protégé documentation for the details on how to create class, subclasses and slots.

Pepper Ontology
In the pepper ontology, spices of pepper are defined. The conceptualization is defined in way that each member of a pepper family can be identified as a sweet pepper or black pepper. The pepper can be affected with some diseases or attacked by some insects.



7. CONCLUSION

It is quite clear that ontology development is necessarily an iterative process. Among several viable alternatives, we will need to determine which one would work better for the projected task, be more intuitive, more extensible, and more maintainable. We also need to remember that ontology is a model of reality of the world and the concepts in the ontology must reflect this reality. We have described a tool-assisted method for building the basis for ontologies adopted from domain analysis.

The ontologies built by this method may not yet be comprehensive or formal enough for some purposes but they provide sufficient information and concepts to facilitate the task of ontology coding and formal documentation.

The hardest part is designing a good ontology before implementing it with Protégé. Working with Protégé to generate OWL is much easier and faster than conventional programming. Once you have a design, implementing it in Protégé only takes hours. The goal is to create learning ontologies that respond to changes in the environment.

8. FUTURE WORKS

The research presented in this thesis is not the terminus. The following future works that can be done to the present work are listed below:

- Extend the ontology by including the treatment of diseases that can affect the classes of both black and sweet pepper.
- Include the various methods that can be used to control insects that can attack species of pepper.
- It is possible to extend the ontology by attaching a reasoning plug-in architecture based on first order logic.

REFERENCES

[1] T. Berners-Lee, J. Hendler, and O. Lassila (2001) The semantic web. Scientific American, May 2001.

[2] Gruber R. (1993) Formal Ontology in Conceptual analysis and Knowledge Representation. Chapter "Towards principles for the design of ontologies used for knowledge sharing"in Conceptual Analysis and Knowledge Representation.

[3] Chandrasekaran B, Josephson JR and Benjamins VR. W (1999) Are ontologies and why do we need them? IEEE Intelligent Systems; 4(1):20-26

[4] Baader F, Calvanese D, M Schneider P. (2003). The Description Logic Handbook. Cambridge University Press. 2003.

[5] BORST, P., BEAKKERMANS, H. (1996) "An Application of Ontology Construction", ECAI-96 Workshop on Ontological Engineering, Budapest, August 13th.

[6] FERNANDEZ, M., GOMEZ-PER (1997) "METHONTOLOGY: From Ontological Art Towards Ontological Engineering", AAAI-97 Spring Symposium on Ontological Engineering, Stanford University, March 24-26th.

[7] USCHOLD, M. and KING, M. (1995) "Towards A Methodology for Building Ontologies", IJCAI-95 Workshop on Basic Ontological Issues in Knowledge Sharing, Montreal, Canada.

[8] USC "Ontologies: Principles, Methods and Applications", Knowledge Engineering Review, **11**(2), 93-137.

[9] VAN DER VET, P.E. and MARS, N.J.I. (1999) Construction of Ontologies: The Case of an Ontology of Pure Substances", Technical Report 95-35, Department of Computer Science, University of Twente, Netherlands.

[10] GOMEZ-PEREZ, A., FERNANDEZ, M. and DE VICENTE, A.J. (1996) "Towards a Method to Conceptualize Domain Ontologies", ECAI-96 Workshop on Ontological Engineering, Budapest.

[11] GOMEZ-PEREZ, A., (1997). "A Framework to Verify Knowledge Sharing Technology", Expert Systems with Applications, **11**(4), 519-529.

[12] GR_ NINGER, M. and FOX, M.S. (1994a) "The Design and Evaluation of Ontologies for Enterprise Engineering", Workshop on Implemented Ontologies, European Conference on Artificial Intelligence 1994,, Amsterdam, NL.

[13] N. Fridman Noy, R. W. Fergerson, and M. A. Musen. The knowledge model of Prot´eg´e-2000: combining interoperability and flexibility. SMI technical report, Stanford University, School of Medicine, 2000. Submitted for publication.

[14] M. R. Genesereth and R. E. Fikes. Knowledge interchange format version 3.0 reference manual. Report Logic 92-1, Logic Group, Stanford University, California, 1992.

[15] W. E. Grosso, H. Eriksson, R. W. Fergerson, J. H. Gennari, S. W. Tu, and M. A. Musen.Knowledge modeling at the millennium: The design and evolution of Prot´eg´e-2000. In 12th Banff Workshop on Knowledge Acquisition, Modeling, and Management. Banff, Alberta, 1999.

[16] D. L. McGuinness and F. v. Harmelen, "OWL web ontology language overview: W3C recommendation 10 February 2004", OWL Web Ontology Language, W3C, 2004.

[17] J. Gennari, M. Musen, R. Fergerson, W. Grosso, M. Crub´ezy, H. Eriksson, N. Noy and S. Tu, "The evolution of Protégé 2000: An environment for knowledge-based systems development", International Journal of Human Computer Studies, 2003, 58(1):89–123.

[18] OWL Web Ontology Language http://www.w3.org/TR/owl-features/

[19] Fox, M. et.al. "An Organisation Ontology for Enterprise Modeling", In *Simulating Organizations: Computational Models of Institutions and Groups*, M. Prietula, K. Carley & L. Gasser (Eds), Menlo Park CA: AAAI/MIT Press, pp. 131-152,1998.

[20] Uschold, M. et.al. *The Enterprise Ontology* The Knowledge Engineering Review , Vol. 13, Special Issue on Putting Ontologies to Use (eds. Mike Uschold and Austin Tate), 1998. Also available from AIAI as AIAI-TR-195 at: http://www.aiai.ed.ac.uk/~entprise/enterprise/ontology.html

[21] http://protege.stanford.edu

Improving Pedagogy in a Digital Signal Processing Course Using Computer-Aided Learning Systems

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ABSTRACT
The development and deployment of a computer-aided learning tool which serves as a learning aid for undergraduate course in digital signal processing is presented. We have carefully outlined the construction of the algorithm and the implementation process of the software with the aim of improving the level of understanding and assimilation of the concepts that make up the course. It also inspires software development at undergraduate level. Although the scope of this project was limited to fundamental principles of Digital Signal Processing, it was found to inspire software development among undergraduate students.

Keywords: Simulation; Computer-aided learning; Digital Signal Processing, CASdsp

1. INTRODUCTION

Digital Signal Processing is at the heart of modern development. Its advantages include: Smaller dimensions in designing, higher Reliability, better capability in complex processing and lower price of communication equipment. The demand on modern communication equipment is ever increasing. For example, the computers have brought with them, greatly expanded requirements on systems as well as on the already crowded radio frequency spectrum.

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It is not surprising therefore that there have been considerable intents in Digital Signal Processing (DSP) to improve performance, testability and flexibility. Despite the promises of DSP in the area of promotion of technological development, especially in developing countries like Nigeria, the opportunities provided by adequate manpower development in this field of study has often eluded these nations. This problem stems from inadequate training received by professionals in this field. This project is aimed at providing a learning tool that will curb the advancement of this trend in a country like Nigeria where there is not only a dearth of manpower in this field, but also inadequate experimental tools to aid the understanding of students and trainee engineers [1, 2].

The problem we seek to alleviate is a complicated one that took its root from the facts that there are too few available resources for learning the concept of Digital

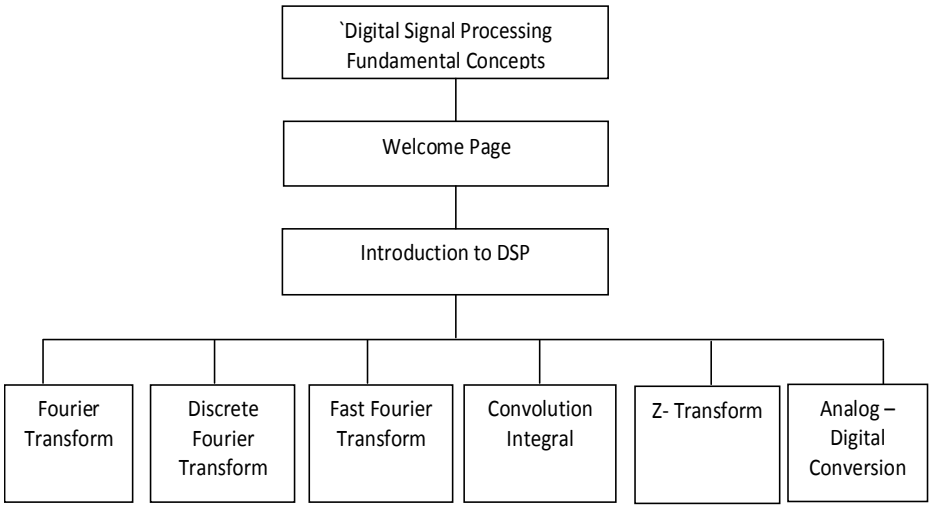

Figure 1: Modular Design of the Complete System

Signal Processing thoroughly in schools; non-availability of the microchips designed to Digital Signal Processing in most electrical college laboratories; scarcity of efficient software to handle the concepts; a high student to lecturer ratio in most of the higher institutions that offer this course

This project also aims at providing the opportunity for indigenous software development in Nigeria by motivating students to embrace software development activities as computer-aided systems similar to these are being implemented all over the world [3, 4, 5]

2. System Design and Algorithm Development

In order to develop a truly effective computer aided system for teaching and learning system (CASdsp), the various concepts in Digital Signal Processing (DSP) are broken down into modules in accordance with the top-down modular programming technique [6]. The main concept behind CASdsp is developed by writing program codes and building user interfaces in groups. Each of these groups or 'building blocks' which form the modules possess other functions which are carried out or executed within that particular group and sometimes infers relevant data from other groups within the system to carry out its commands. Each of these modules is created such that each contains a set of related, interconnected and sometimes interdependent instructions or commands. Once these sets of modules have been developed, the software package was then created by integrating these different modules such that each module can be accessed, upon user request by another module. The developed software has six main modules; each of these modules has sub-modules. The modular breakdown structure of the Computer Aided Learning System for DSP fundamental given the opportunity to read a brief introduction to the concept of Digital Signal Processing under the caption "Introduction".

concepts is shown in Fig 1. Each module was then further broken down into three segments as explained below:

2.1 The Input Interface

The input interfaces were designed to receive system parameters as designed for the algorithms developed. These interfaces were designed specially to be very sensitive to errors such that the user will be guided as to which form, type and nature of data are applicable to the concept being handled.

2.2 The Processing Engine

This sub-module is dedicated to working out the solution to the problem created using the input parameters and carrying out specific operations as indicated in the algorithm developed for that module. The results emanating from the calculations and operations performed are then sent to the output interface for display.

2.3 The Output Interface

Results obtained from the operations of the processing engine are sent here for display. This sub-module is closely linked with the input interface displaying parameters entered by the user as input, the results generated after processing and then the graphical representations of the output.

3. SYSTEM IMPLEMENTATION

The implementation of the design was done using the Microsoft Visual BASIC Integrated Development Environment to make it user user-friendly [7], therefore, the CASdsp uses an event-driven, object–oriented programming language. Shown in Figure 2 is the main menu of the developed software and sample results of some of its modules: On this form, the user (the student) is

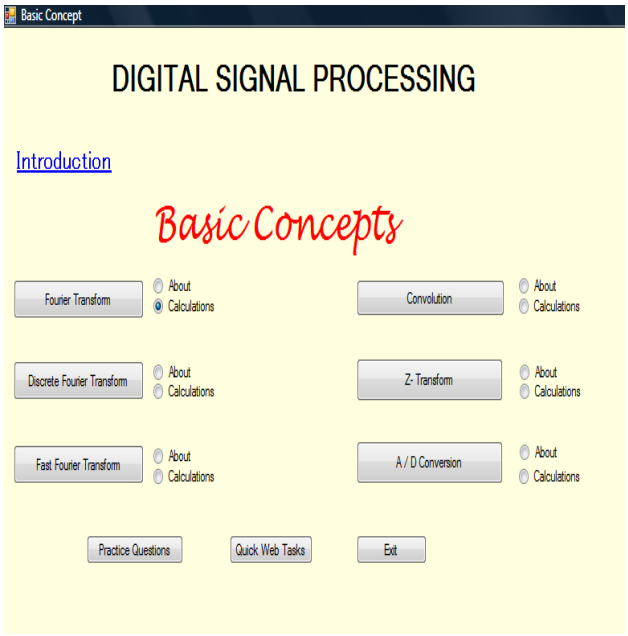

Figure 2: Main Menu of the Developed package

Then one can proceed to know about each of the fundamental concepts by clicking on the "about" radio button and then clicking on the desired concept. The program is very user – friendly and designed specifically with the undergraduate curriculum in mind such that important issues under each of the concepts are displayed at the request of the user, ranging from origin of the concept to the applications of concepts in real life problems as well as examples and practice questions on the concept selected.

All these are put in place in other to give the student sound background knowledge of the concept. Then, to practice what has been read, another interface was developed where the user can apply some of the principles learnt from the theoretical knowledge
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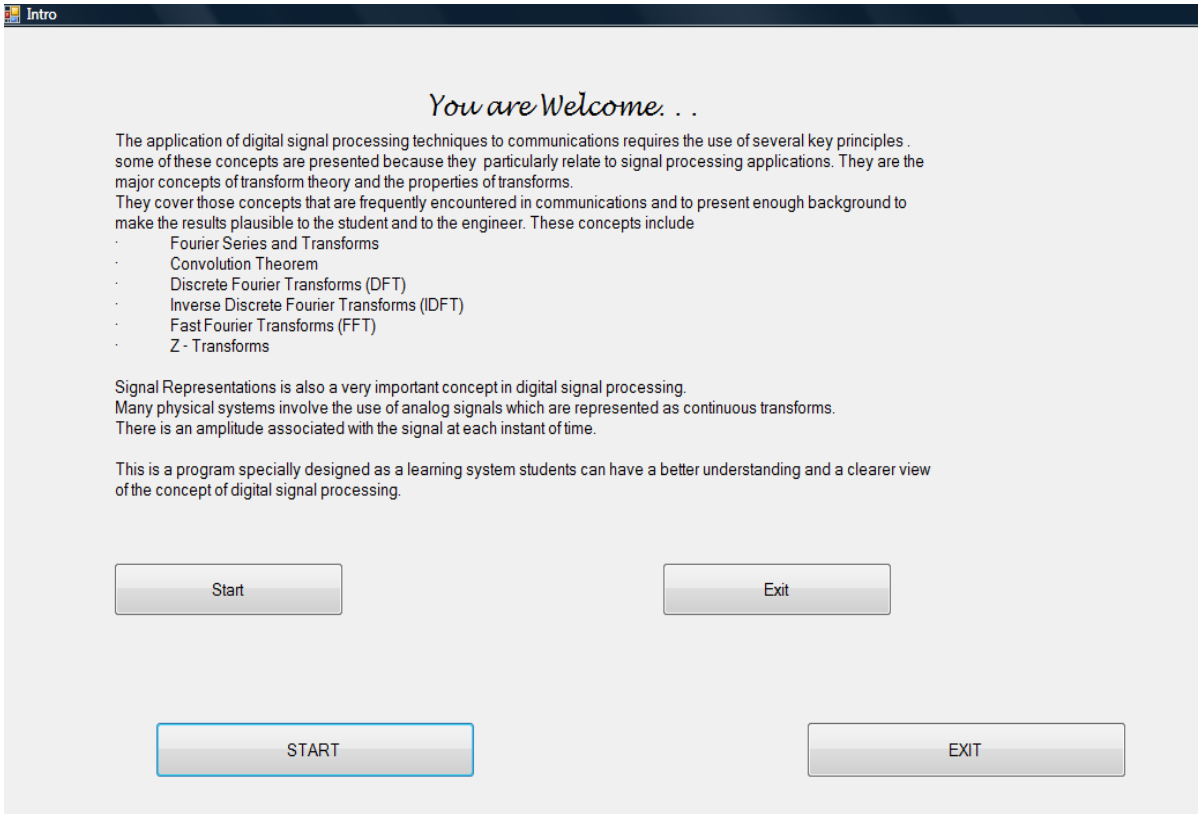

Figure 3: Introductory Page to Digital Signal Processing Concepts

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3.1 Fourier Transform Module

Fourier Transforms are primarily used to represent finite-length analog signals [8, 9, 10], although they can be used to represent some continuous signals such as sin (wt) and $e^{jwt.}$

On clicking on the "Calculation" radio button and clicking Fourier Transform button, the main menu window is unloaded and message box appears prompting the user to select the time format. The form shown in Figure 4 for example, is the window which comes up when "Continuous Time" is chosen as the time format "Exponential function" has been selected as well on this form as the type of input. On selection of the type of input, a textbox appears which enables users to enter the amplitude and period of the function selected. The software calculates the Fourier transform and displays the output in frequency domain when the "Transform" button is clicked. Also a graphical representation of the input signal coming in time domain and the output signal graph coming in frequency domain is displayed when the "Plot Graph" button is clicked. This enables the user to view the graphical representation of the type of input as well as the characteristics of the function that was entered as well as the properties of the frequency function coming as the output after being transformed using Fourier Technique

All these can be seen in Figure 4. Other types of input that the user can access are Fourier series and Complex Fourier Coefficient which also give, as output, the function in frequency domain as well as the graphical plot of the input and output functions. All these can also be done in discrete format if the user selects the "Discrete Time" format when prompted.

3.2 Discrete Fourier Transform Module

The Discrete Fourier Transform is the parallel of the continuous Fourier transform for sampled data system [8]. The input parameter window enables users to enter the various time – domain functions to be transformed into frequency domain functions. The software is designed to give allowance of, as much as, four different input signals [x(n)] and their ranges at a time. The number of points to be used for the computation of the DFT is also entered by the user. The software also gives the user the opportunity to view the graphical representation of each of the input signal independently as the functions are typed in even before the individual functions are transformed. This is shown in Figure 5. Then, on clicking "Transform", the output, which is the frequency domain equivalent of the function typed in, as input, is displayed and a graphical representation of the output is displayed alongside. This is shown in the Figure 6.

3.3 Fast Fourier Transform Module

Fast Fourier Transform algorithms (FFTs) collectively form an enormous number of fast algorithms for the computation of the DFT [8, 9]. The most popular types which are the ones used in this program are the Radix -2 algorithm and the Radix -4 algorithm which both come with decimation in time and decimation in frequency.

On clicking on the "Fast Fourier Transform" button on the Basic Concepts Menu window, after indicating "Calculation" on the radio button, a message box asking which FFT format to be used pops up. On this message box are two options: Radix – Two and Radix – Four. The form shown above is the result of clicking on Radix – Two and on this form input parameter window for Radix-Two FFT calculation. Here, the user is given the allowance to input as many as four separate and independent equations representing functions in the time domain x(n) with n = 0, 1, . . . (N/2) -1. Also, the period for the time-domain functions N is as well required as an input. A privileged opportunity -is then given to the user to view individually and independently the graphical representation of each of the input functions entered in line with the period (*N*) entered. All these are designed by the programmer to make the CALS as user-friendly as possible. This gives the user an idea of the characteristics of the input signals. This is shown in Figure 7

The form shown in Figure 8 displays the result obtained when the 'Transform' button is clicked by the user to get result of the transformation of the input, time-domain functions to frequency – domain functions as the output. The result is shown in the space provided for the output just below the input and a butterfly representation showing how the result was obtained is displayed immediately just alongside the result as shown in the Figure 8. If the Radix Four FFT algorithm is selected, then the Radix Four FFT algorithm window as shown in Figure 9 pops up. In this window, the user is allowed to enter 16 various input parameters that come as time domain functions *x*(n). the number of FFT points is to be entered by the user. The result is that, as shown in Figure 8, where the program computes the FFT of the functions entered and displays the results individually just to make the user see in a well defined form the result of each of the individual functions *g*(1) to *g*(16). Afterwards, a butterfly representation to explain how each of the results were computed is displayed when the user clicks on "Details". This is shown in Figure 4.

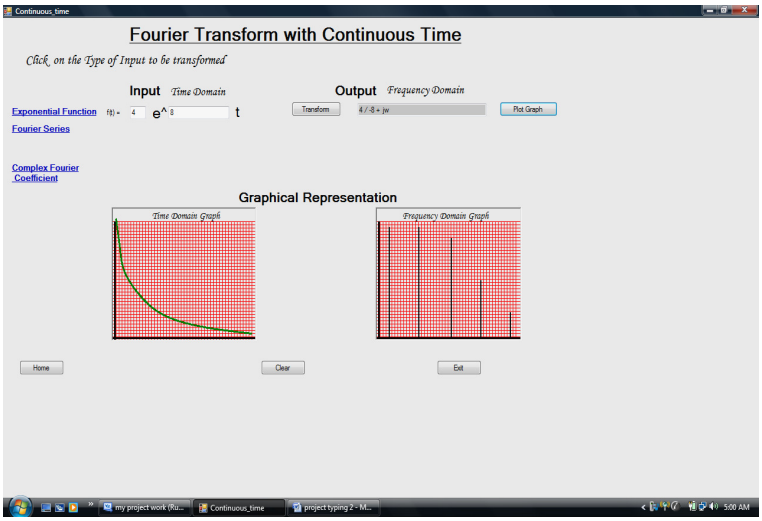

Figure 4: Sample result of Fourier Transform Module

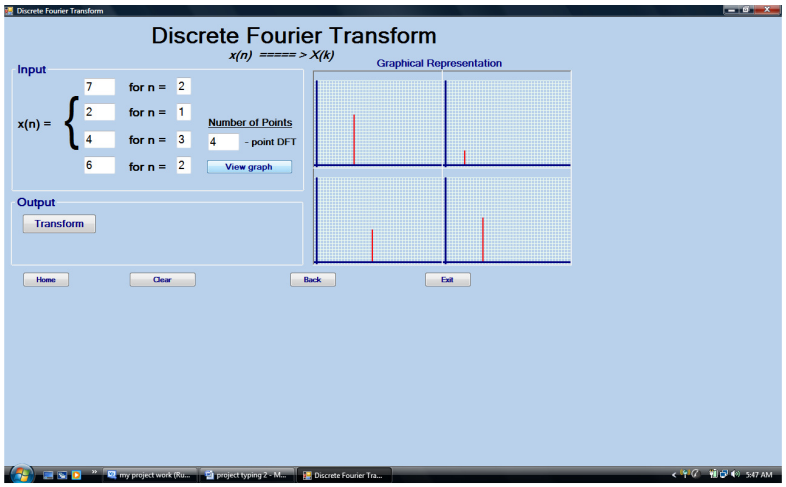

Figure 5: Input Parameter Window for Discrete Fourier Transform

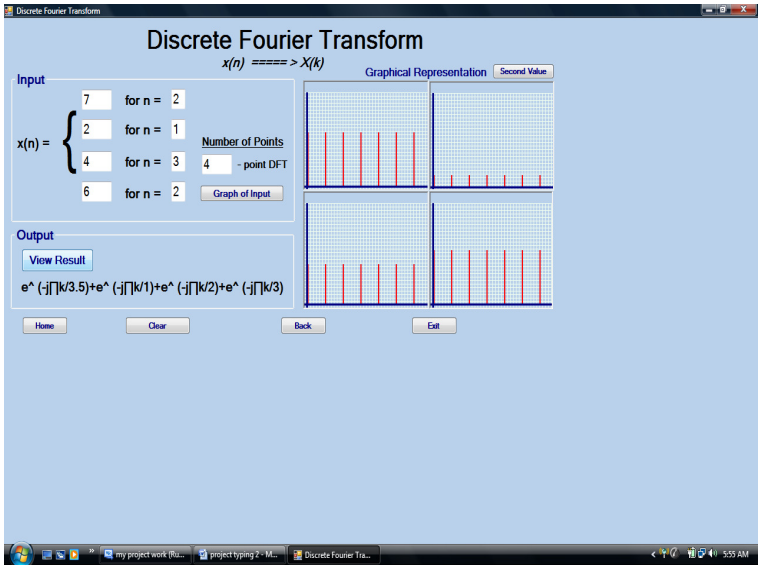

Figure 6: Sample result of the Discrete Fourier Transform Module

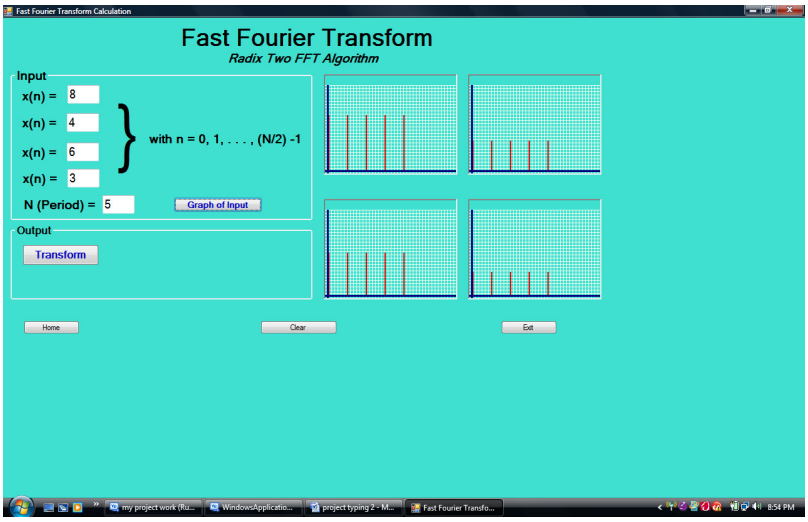

Figure 7: Input Parameter Window for Fast Fourier Transform

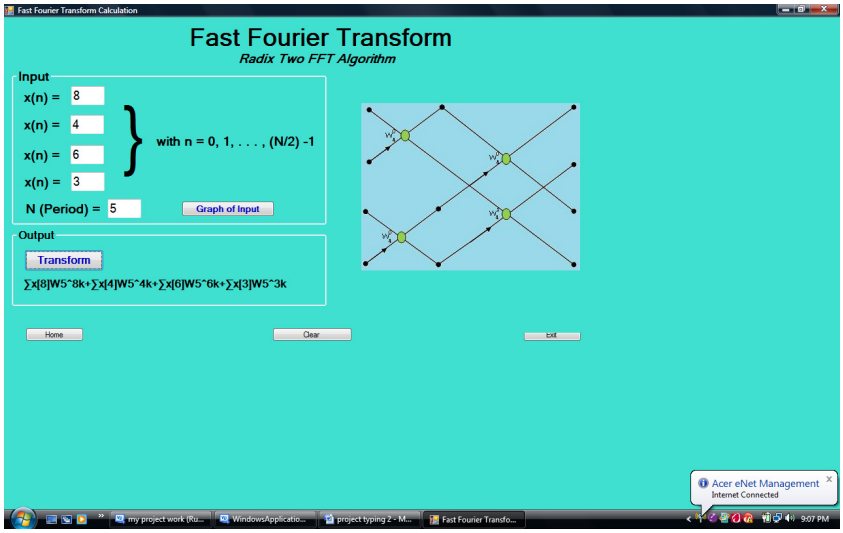

Figure 8: Sample result of the Radix two Fast Fourier Transform Module

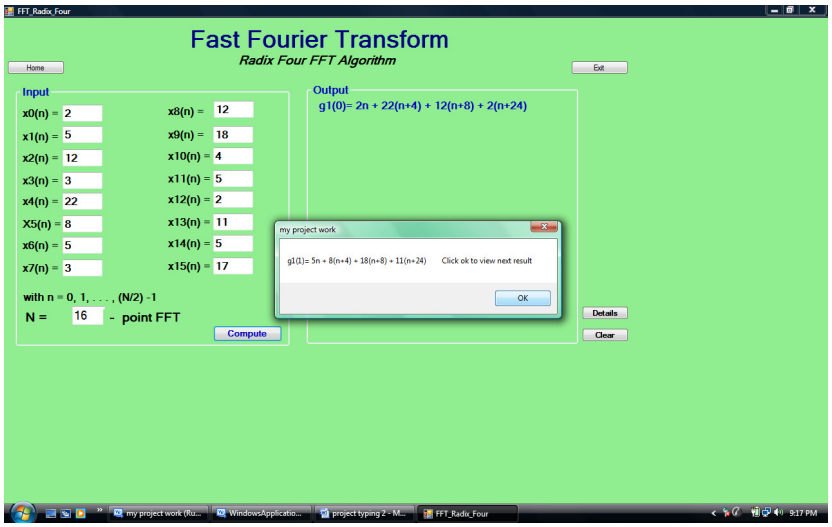

Figure 9: Radix Four FFT algorithm window

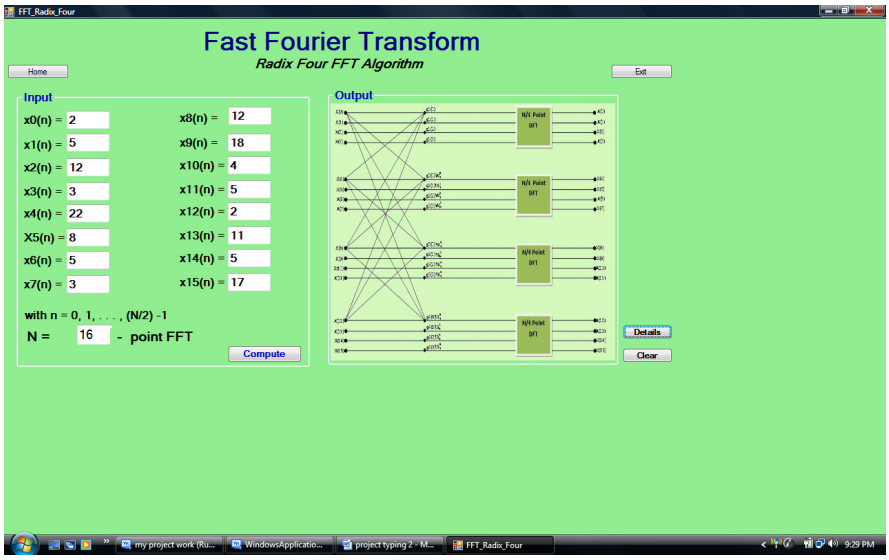

Figure 10: Sample result of the Radix Four FFT module

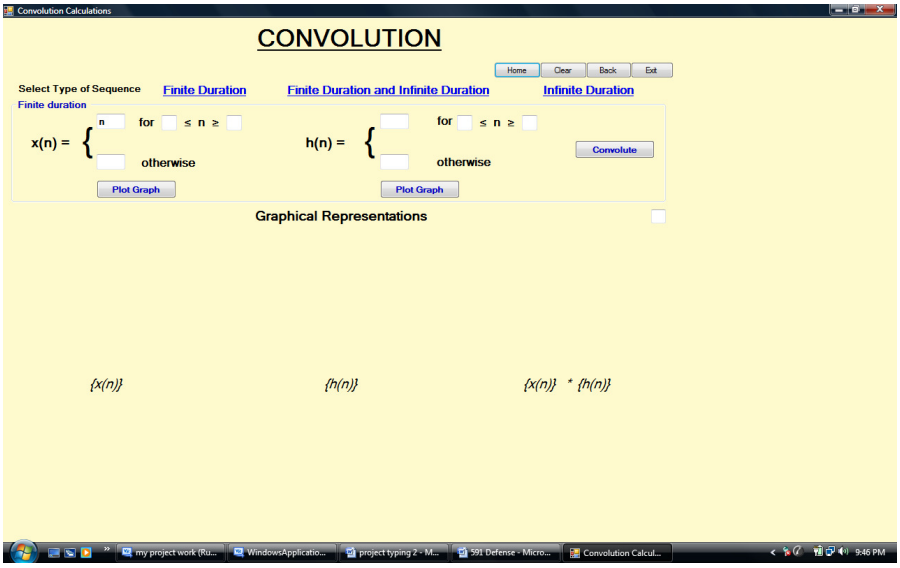

Figure 11: Input parameter window for Convolution Integral

3.4 Convolution Module

Convolution helps to give the result of the intersection of the region of convergence of analog input [7]. This comprises of the concept definition and explanation part as well as the module where the knowledge gained can be applied in form of calculations. Clicking on "Convolution", after selecting "Calculation" on the radio button, loads the convolution calculation window where the user can first select the type of sequence desired. We can view the individual plot of the input parameters, in form of graphs, even before convolution takes place.

The result of the convolution as well as the graphical representation of the region of intersection is also shown in Figure 12.

The result shown in Figure 12 is a sample of the output obtained when 'infinite duration' is selected as the type of sequence and the input parameters representing the analog inputs are entered in form of x(n) and h(n). Individual graphs representing the domain of x(n) and h(n) respectively is displayed immediately the "Plot Graph" button is clicked by the user. The result, as well as the result of the intersection, is displayed when the user clicks on "Convolution" button

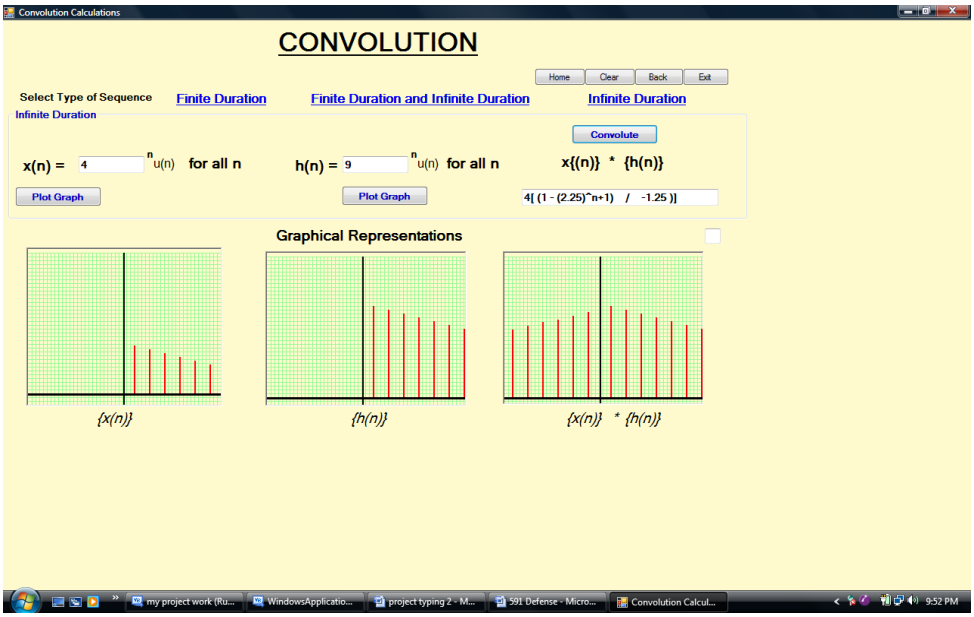

Figure 12: Sample result of the Convolution Integral module

3.5 Z- Transform Module

The Z –transform is only defined for the regions of the complex plane in which the summation on the right converges [6]. Very often, the signals start at n=0, that is, they are nonzero only for $n \geq 0$. If the user clicks on 'Z-Transforms' after checking the radio button for 'Calculation', the Z-transforms window for calculation pops up, which gives the user the opportunity to select different types of input to be transformed such as discrete unit pulse, step function, unit pulse shifts, exponential function and trigonometric function. The student is thus given the opportunity to select one type of function at a time. Then, the user enters the function applicable to the type he has chosen. On clicking the 'transform' button, the result of the transformation is displayed as well as a graphical representation of the input.

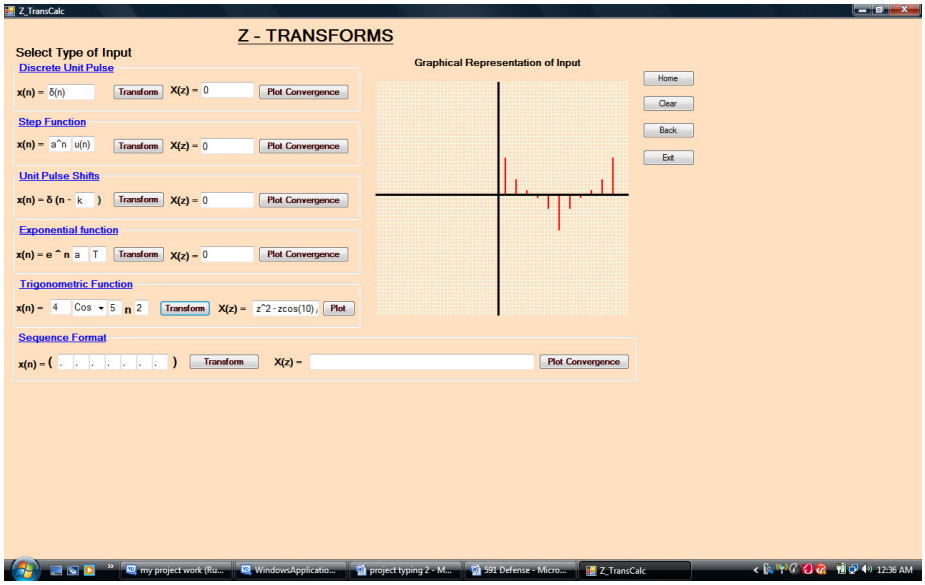

Figure 13: Input Parameter Window for Z-Transform

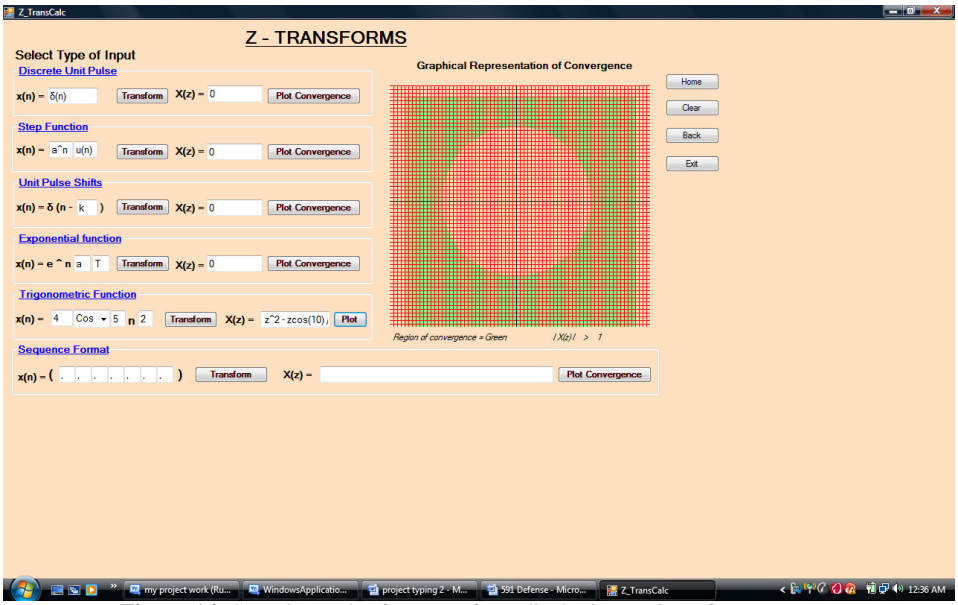

Figure 14: Sample result of Z-Transform displaying region of convergence

3.6 Analog – Digital Conversion Module

Basic Processes involved in analog to digital signal conversion are, anti-aliasing, sampling, quantizing, encoding [5, 6, 7]. The introductory section is where the user can read about the basic processes involved in the conversion of analog signals to digital signals. On clicking the corresponding button for each of the concepts underlined, more explanation on each of these concepts are displayed for the user to read and learn. A sample is shown in Figure 15.

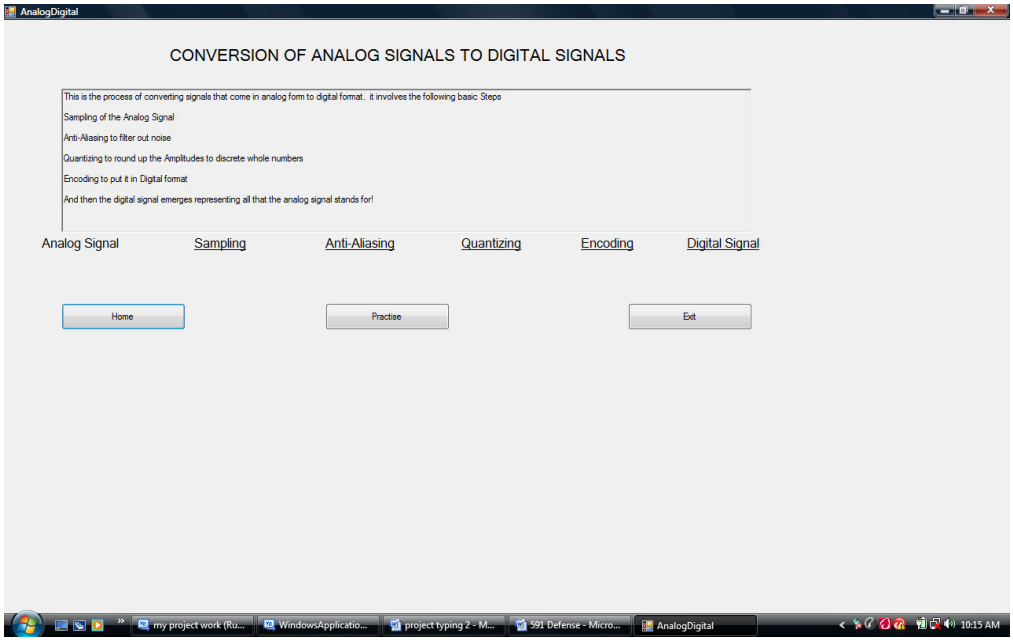

Figure 15: Introduction Module for Analog to Digital Conversion

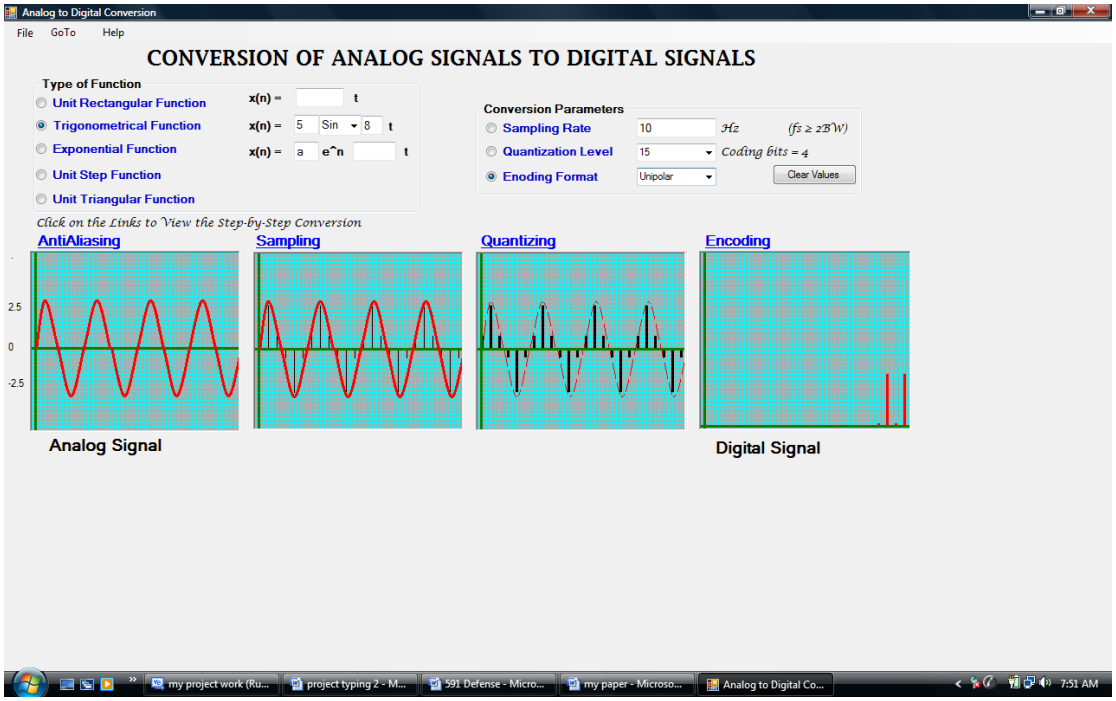

Figure 16: Sample result of Analog to Digital Conversion Module

When the user is ready to implement the knowledge learnt, he clicks on 'A-D Conversion' after marking the 'calculation' radio button. The window for Analog to Digital Conversion pops up. Here, the user can first select the type of function: ranging from unit rectangular function, trigonometric function, exponential function, even to unit step function, among others.

Then he enters the input (analog) signal, the sampling rate, to determine the amplitude at each point of the continuous signal and then enter the quantization level. Once the quantization level is selected, the bit resolution is displayed as applicable to the selected level. The encoding format, whether bipolar or unipolar coding, is then selected. Thereafter, the student clicks the various stages of the conversion to see what graphical representation at each stage of the conversion looks like.

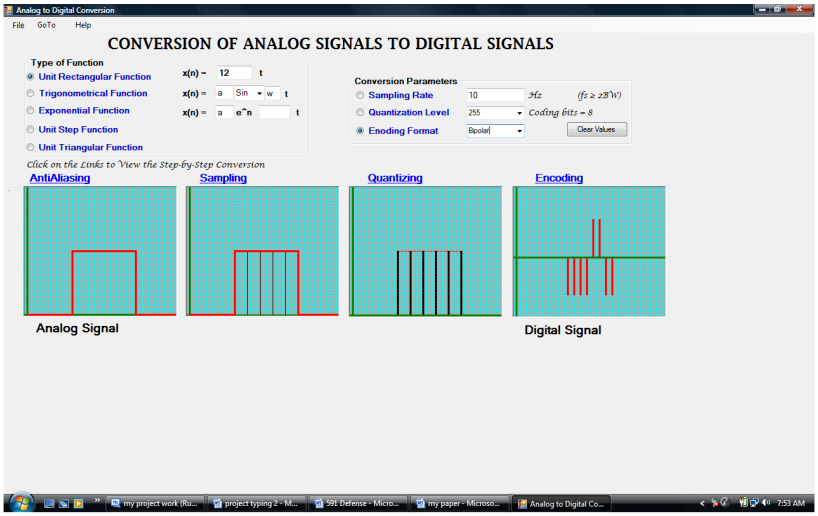

Figure 17: Sample result of Analog to Digital Conversion using unit rectangular function

4. DISCUSSION

After the successful completion of the design implementation stage, the software was compiled into an executable file and currently runs as a stand-alone application pending the time it will be deployed on some systems in the Department of Electrical Engineering, University of Ilorin. The software is presently undergoing scrutiny and criticism from users which will enable it to be improved based on the response and reaction of the users after their interaction with the software. Modifications can be done to meet up with users' expectation of the program. The deployment was done on systems running Microsoft Vista and Miscrosoft Windows XP.

5. CONCLUSION

Obviously, our tertiary learning institutions require better training and learning facilities to cope with the fast rate of technological advancement in this age and time. Since computers can now be easily afforded by these institutions, it is pertinent that we seize the opportunity to develop computer aided learning systems which will aid better and faster learning as well as efficient teaching in the classroom. The pace of learning can be controlled and improved and this also means that students can make better and more intelligent choices in what and how to learn, skipping unnecessary items or doing remedial work in difficult concepts, all with aim of understanding better and faster. Such control makes students feel more competent in their learning.

As regards this project, there is still more work to be done in the other areas and aspects that make up the concept of Digital Signal processing and there are already interesting developments in the pipeline. The program would be upgraded with time to suit the needs, desires and convenience of the user as well as to make a more efficient learning package and an apt teaching tool. This software is adjudged to have solved the problem of enabling the students grasp better, the basic concepts of digital signal processing thus satisfying the objective.

Just like every other software developed, it has its limitations part of which is the fact that the scope is limited to just the fundamental principles in DSP and it is designed for training in institutions of learning not as a replacement for microcontrollers used for digital signal processing in equipments and appliances. Experts can however make use of it to further train interns and apprentice who have at least a good background in the field.

REFERENCES

[1] M Nwadiani and N.E. Apotu (2002): *Academic Staff Turnover in Nigerian Universities*; Education, Vol. 123.

[2] B. Oni (1999): *The Nigerian University Today and the Challenges of the Twenty-first Century*; Monograph, No. 60. Institute for World Economics and International Management, University of Bremen, Bremen, Germany.

[3] M.W. Goldberg (1997): CALOS: first results from an experiment in computer-aided learning for operating systems, Proceedings of the twenty-eighth SIGCSE technical symposium on Computer science education, NY, USA,

[4] P.S. Goodman (1998): Computer-Aided Systems and Communities: Mechanisms for organizational learning in distributed environments; Management Information System Quarterly, University of Minnesota, (22) 4.

[5] J.N. Hudson (2004): Computer-aided learning in the real world of medical education: does the quality of interaction with the computer affect student learning?; Medical Education, (38) 8, pp 887 – 895.

[6] A.V. Aho, J.E. Hopcroft and J.D. Ullman (1974): The Design and Analysis of Computer Algorithms; Addison-Wesley Publishing Company, Essex, England.

[7] G. Brassard and P. Bratley (1996): Fundamentals of Algorithms; Prentice Hall, New Jersey, USA.

[8] S.K. Mitra (2005): Digital Signal Processing: A Computer-based Approach (Third Edition); McGraw-Hill Series in Electrical and Computer Engineering; McGraw-Hill Higher Education.

[9] J.G. Proakis, D.G. Manolakis (1996**):** Digital signal processing: Principles, Algorithms and Applications (Third edition); Pearson Prentice Hall, New Jersey

[10] P.S.R. Diniz, E.A.B. Da Silva, S.L. Netto (2002): Digital signal processing: system analysis and design; Cambridge University Press, U.K.

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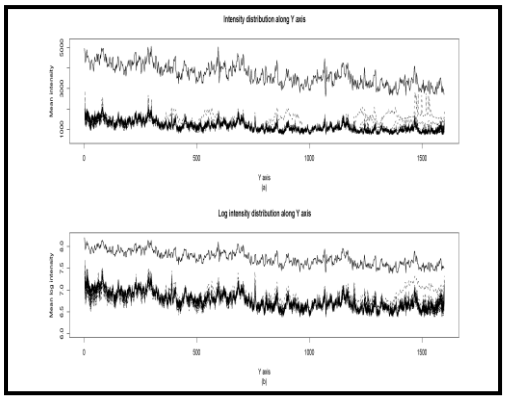

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[2] J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68–73.

[3] I. S. Jacobs and C. P. Bean, "Fine particles, thin films and exchange anisotropy," in Magnetism, vol. III, G. T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271–350.

[4] K. Elissa, "Title of paper if known," unpublished.

[5] R. Nicole, "Title of paper with only first word capitalized," J. Name Stand. Abbrev., in press.

[6] Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, "Electron spectroscopy studies on magneto-optical media and plastic substrate interface," IEEE Transl. J. Magn. Japan, vol. 2, pp. 740–741, August 1987 [Digests 9th Annual Conf. Magnetics Japan, p. 301, 1982].

[7] M. Young, The Technical Writer's Handbook. Mill Valley, CA: University Science, 1989.

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